

# Quicksilver\_MLK Design

## POWER

AC/BATT CONNECTOR PG 57
BATT CHARGER PG 50

CLK GEN SLG8SP585 PG 5
---------------------------

## SYSTEM POWER

SUS/ RUN POWER SW			
+V5_SUS / +V5_RUN / +V1.5_RUN +3.3V_ALW/ +V3.3A_PCH / +V3.3_SUS / +V3.3_RUN PG 58			
CPU VR +VCC_CORE PG 51	VR +V1.1S PG 52	VR +V1.1S_VTT PG 53	
REGULATOR For DDR3 +1.5V_DDR +0.75V_DDR_VTT PG 54	REGULATOR +5V_ALW +3.3V_ALW_17020 PG 55	LDO +V1.8S PG 56	

Dual/Quad Core CPU  
Intel  
Arrandale / Clarksfield  
(35W 2C/45W,55W 4C)  
(989 rPGA)  
37.5 x 37.5 mm  
PG 6-12

DDR III	DDR3-SODIMM PG 14
DDR III	DDR3-SODIMM PG 15

PCIEx8	MXM CONNECTOR 2 PG 27-28
PCIEx8	MXM CONNECTOR 1 PG 25-26

HDMI	HDMI Connector PG 34
DP-A	
VGA	CRT CONN PG 32
DP-D	eDP Connector PG 29
DP-C	LVDS Connector PG 31
DP-C	Display Port PG 34

Panel Connector  
LVDS

Intel  
Ibex Peak M  
(1071 Pin PBGA)  
27 x 25 mm  
PG 16-24

USB2.0	WiMax Half MINI-CARD PG 38
PCI-E	
USB2.0	
PCI-E	UWB/BT MINI-CARD PG 39
USB2.0	
PCI-E	
USB2.0	
RGMII	

Light FX PG 44, 45
Keyboard BL T/P Module
Head Logo - A
Logo - B
Speaker LED

Express Card	Express Switch RICOH R5538D001 (20 QFN) 4 x 4 mm
--------------	--

Audio/ Express Board 3/3

PHY HANKSVILLE 82577LC (48 BGA) 6 x 6 mm PG 47
--

Magnetic PG 48	RJ45 PG 48
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DELL/FLEX CONFIDENTIAL

ONFI PG 35
------------

SIO ITE ITE8512E (128 Pin LQFP) 16 x 16 mm PG 41
--

FLASH Memory FOR SYSTEM (8 Pin SO8W) PG 16
---

Keyboard PG 43	Touchpad PG 43	CIR PG 42
----------------	----------------	-----------

FLASH Memory 2MB (8 Pin SO8W) PG 42
--

MAX7313 X 3 PG 44
----------------------

USER INTERFACE PG 43
----------------------------

THERMAL SMSC4002 PG 40
---------------------------

CardReader CONN
--------------------

PC Card/1394 RICOH R5U230 (QFN 48) PG 46
---

WebCam+DMIC PG 31	USB2.0
USBx2 PG 36	USB2.0
COMBO CONN USB/eSATA PG 36	USB2.0
SATA - ODD PG 37	SATA2
SATA - HDD1 PG 37	SATA2
SATA - HDD2 PG 37	SATA2
1394 PG 46	

USB x 2	USB2.0
Audio Jack	Amplifier MAX9724A
Audio Jack	Amplifier MAX9724A
Audio Jack	AUDIO IDT 92HD73C (56 LQFP) 9 x 9 mm IHDA
Audio Jack	
Internal Speaker 5Wx2	Amplifier TPA6040A4

Audio/ Express Board 1/3

Audio/ Express Board 2/3

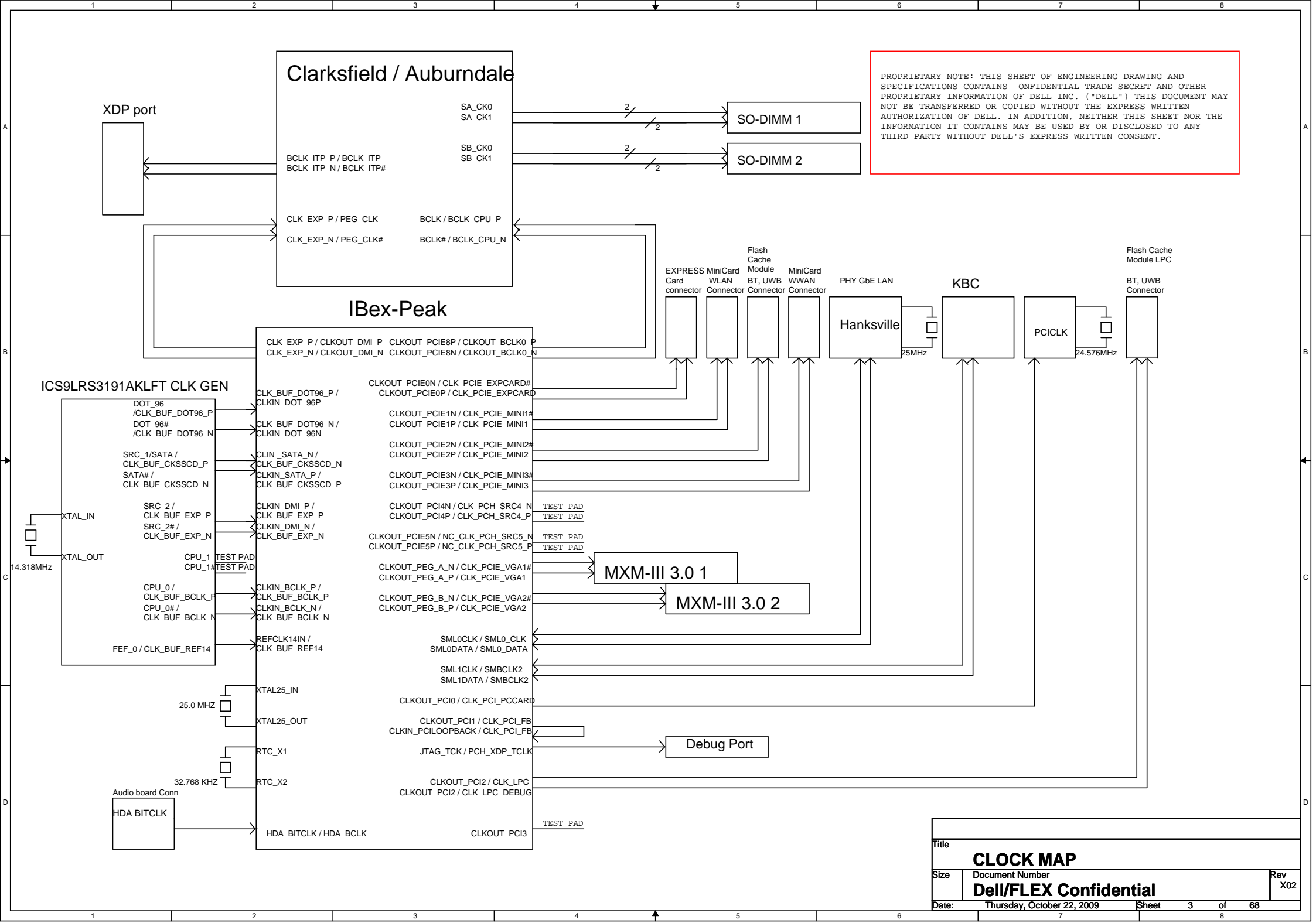
BLOCK DIAGRAM			
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40	FAN & THERMAL EMC4002	66	HISTORY
41	SIO (ITE8512)		
42	FLASH/ RTC/ CIR/ TPM		

Power States									
Power Rail	Control Signal	S0	S3	S4	S5	G3	S4/ M-off	S5/ M-off	
+PWR_SRC	N/A	V	V	V	V				
+0.75V_DDR_VTT	RUN_ON/SUS_ON	V	V						
+V1.1S_VTT	+V1.1S_VTT_MXM1_PWRON	V							
+V1.1S	RUN_ON	V							
+1.5V_RUN	RUN_ON#	V							
+1.5V_DDR	RUN_ON/SUS_ON	V	V						
+V1.8S	RUN_ON	V							
+3.3V_ALW	3VA_PCH_ON	V	V	V	V				
+3.3V_WLAN	AUX_EN_WOWL	V	define WOL	define WOL	define WOL				
+3.3V_RUN	RUN_ON#	V							
+V3.3	SUS_ON	V	V						
+5V_ALW	+5V_EN1/5V_ALW_ON	V	V	V	V				
+5V_ALW2	+PWR_SRC	V	V	V	V				
+5V_RUN	RUN_ON	V							
+5V_HDD	HDDC_EN	V							
+5V_MOD	MODC_EN	V							
+V5S	RUN_ON	V							
+LCDVCC	ENVDD	V							
+RTC_CELL	RTC	V	V	V	V	V			
+VCC_CORE	IMVP_VR_ON	V							
+USB_RIGHT_PWR	USB_SIDE_EN#	V	define	define					
+USB_LEFT_PWR	USB_BACK_EN#	V	define	define					
+15V_ALW	5V_ALW_ON	V	V	V	V				
+3.3V_ALW_17020	+3.3V_EN2/5V_ALW_ON	V	V	V	V				
+V3.3M_LAN	PM_SLP_LAN#	V	define WOL	define WOL	define WOL				

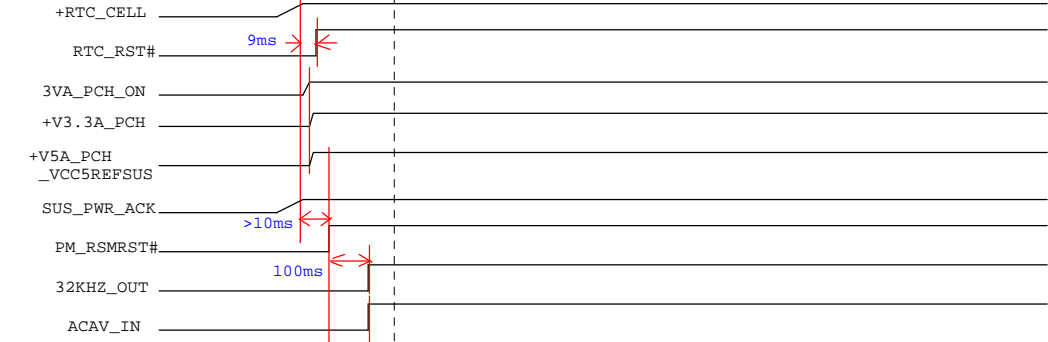
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FRONTPAGE		
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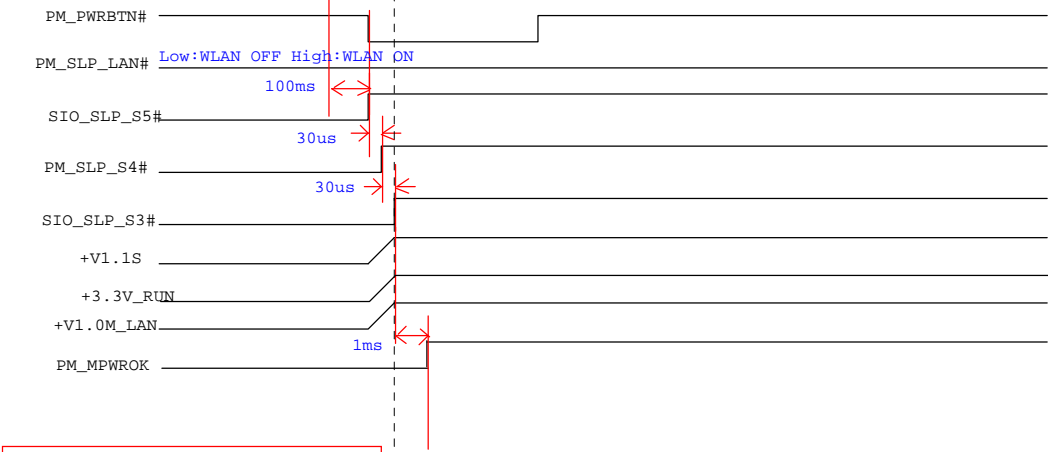


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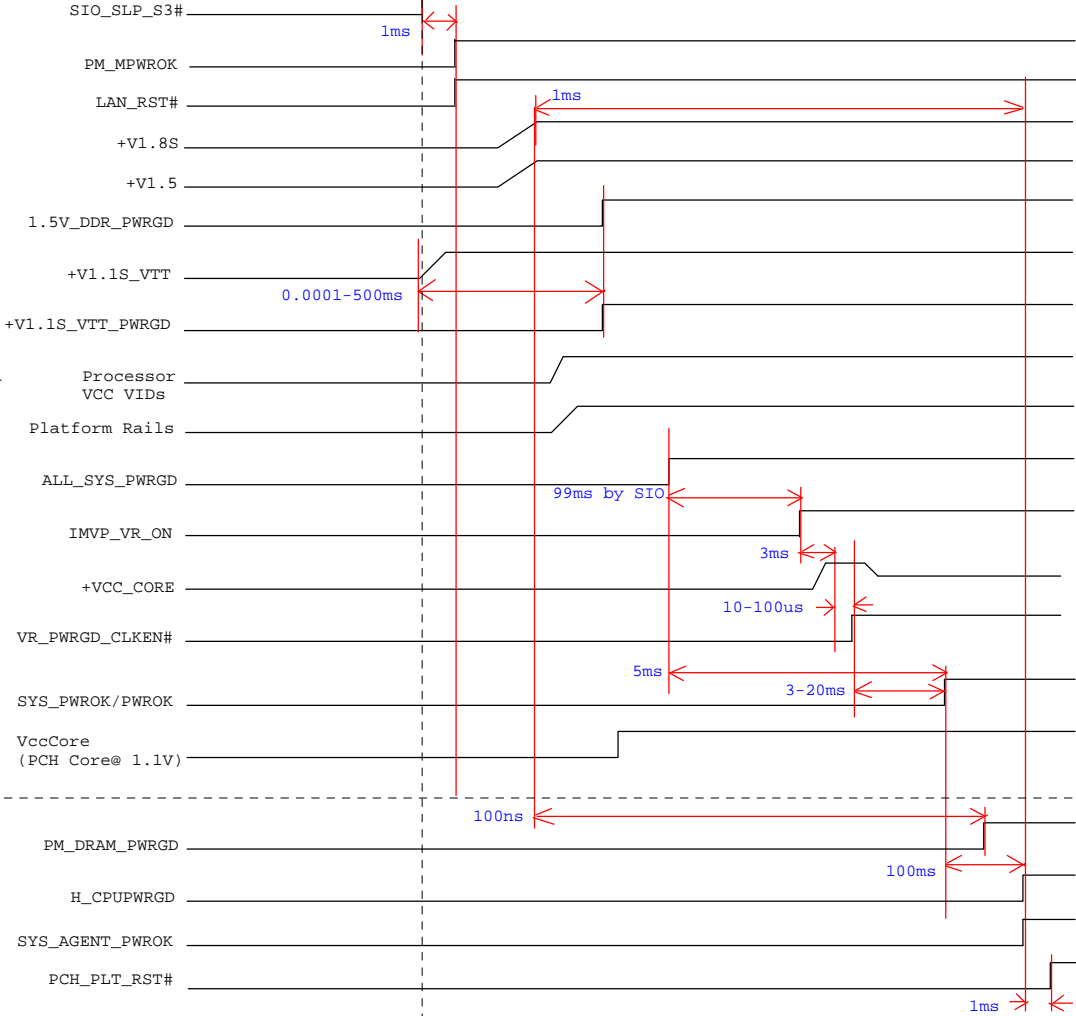
G3 to Sx



Sx to S0

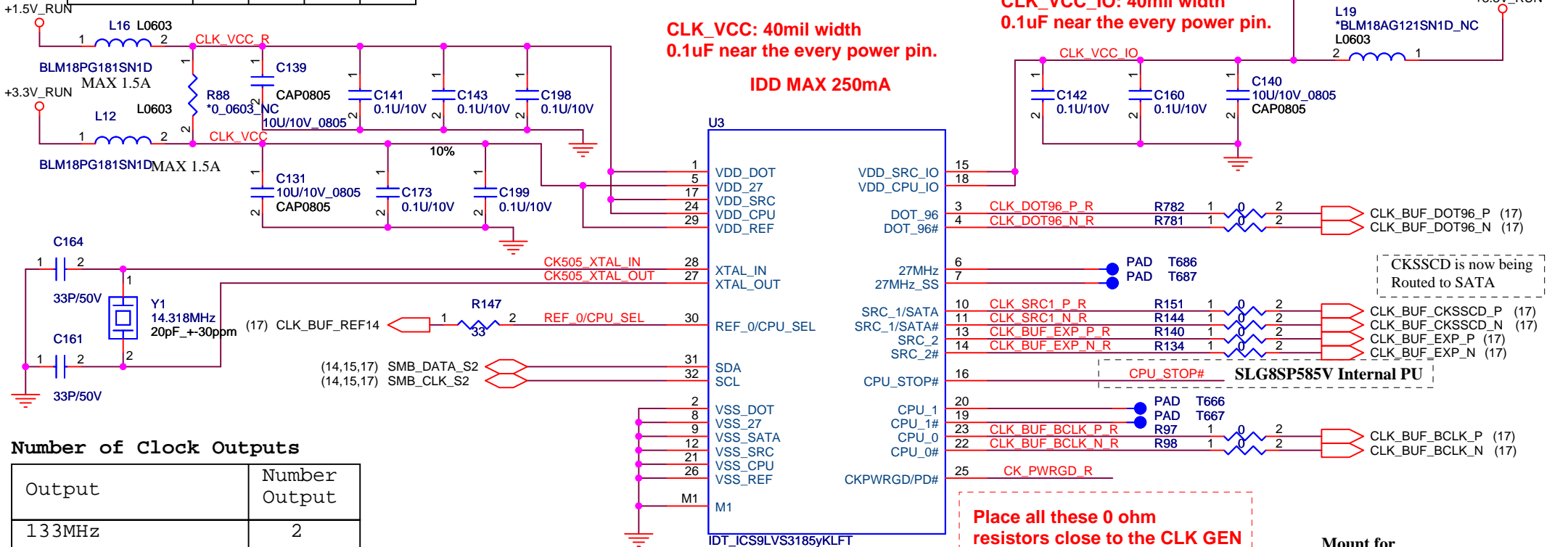
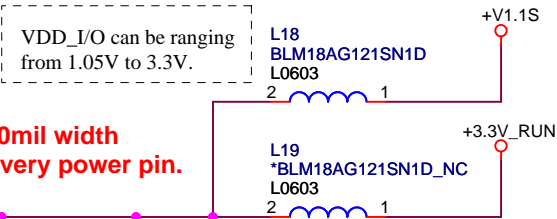


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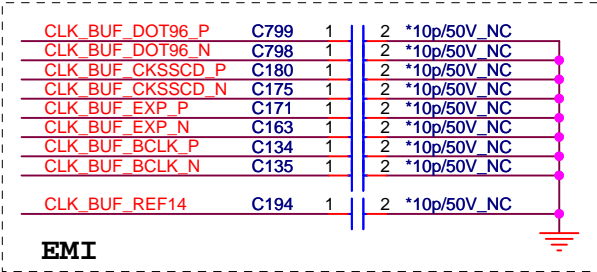
IDT Clock gen	L16	R88	C139	R114
9LRS3191	NA	Add	NA	Add
9LRS3185	Add	NA	Add	NA

	Vender	Vender P/N	FLEX P/N
MAIN	IDT	ICS9LVS3185yKLFT	DELH-12D00J00000006G



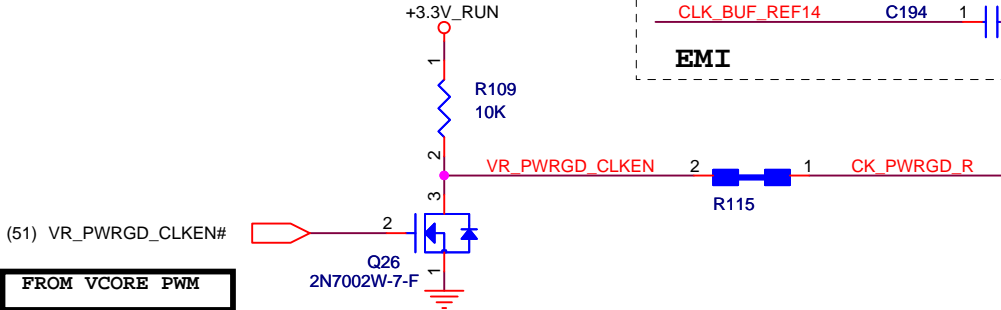
Number of Clock Outputs

Output	Number Output
133MHz	2
SRC(100MHz_SS)	1
SRC/SATA (100MHz)	1
REF (14.3181MHz)	1
DOT_CLK (96MHz)	1
27MHz	1
27MHz SS	1



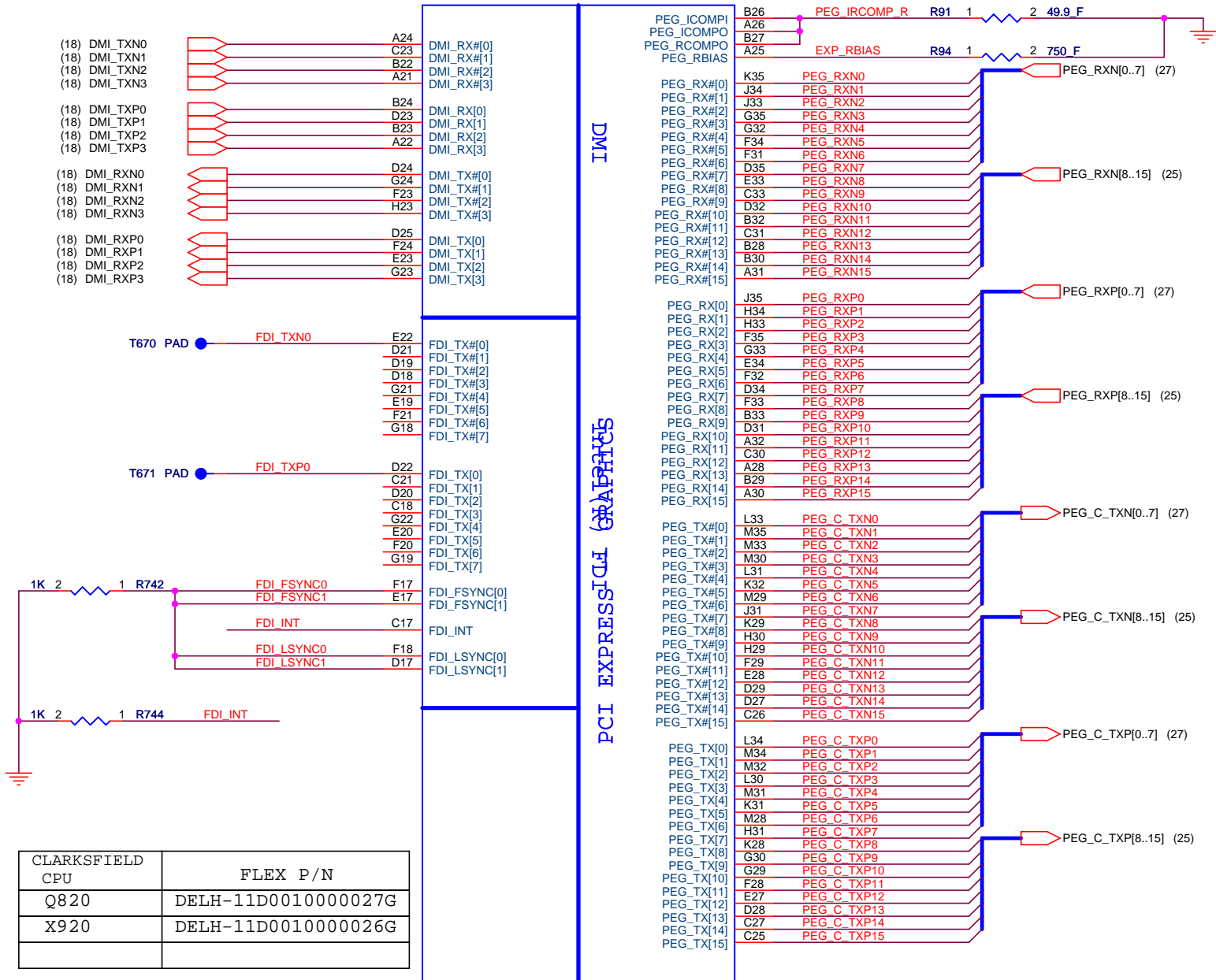
CPU\_SEL During CK\_PWRGD Latch Pin 30

Input (pin 30)	CPU_0/_1	SRC
0 -> NOW	133MHz	100MHz
1	100MHz	100MHz



ARRANDALE /CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

U6A



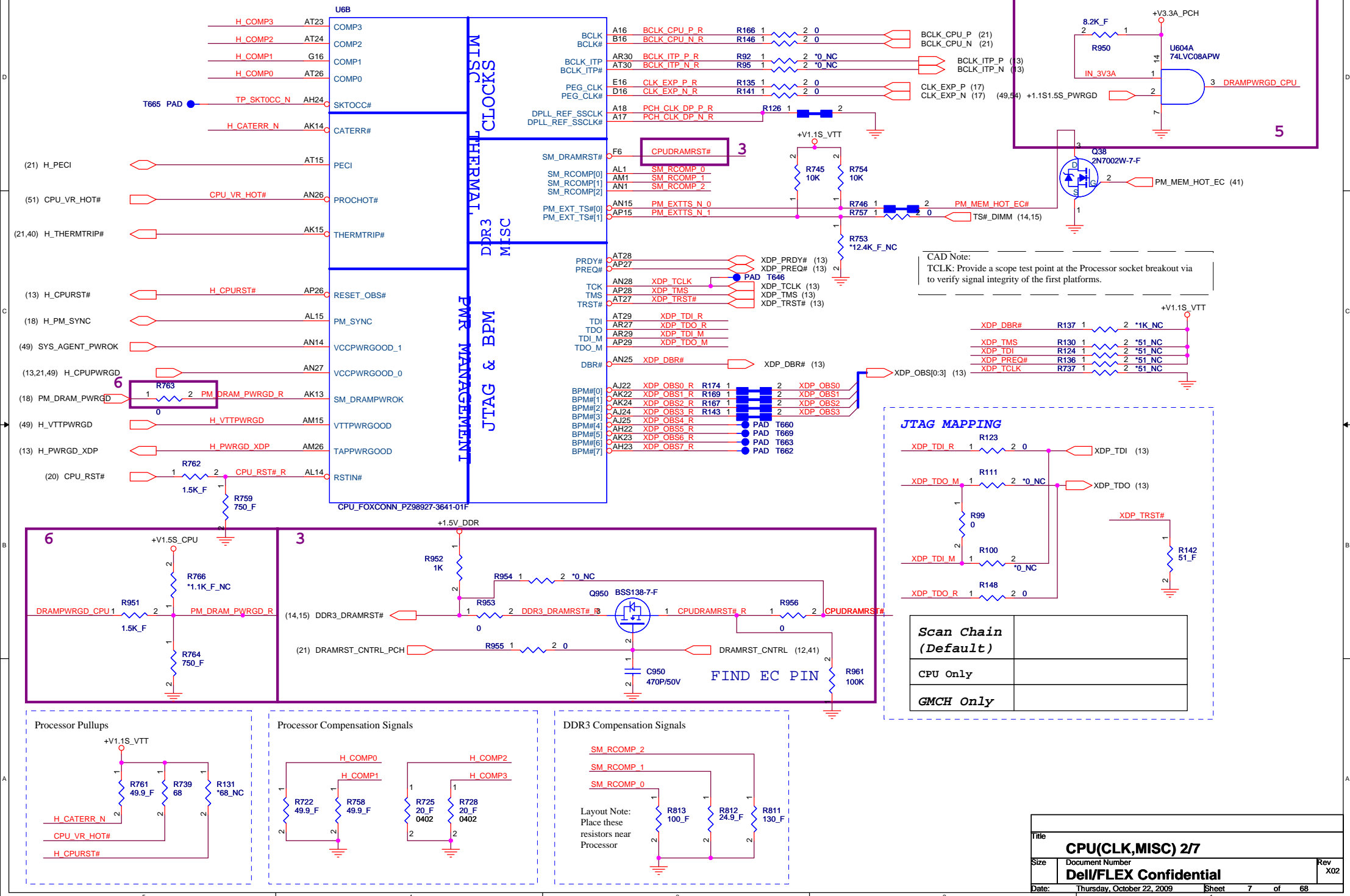
CLARKSFIELD CPU	FLEX P/N
Q820	DELH-11D0010000027G
X920	DELH-11D0010000026G

Arrandale CPU	FLEX P/N
520M	DELH-11D0010000037G

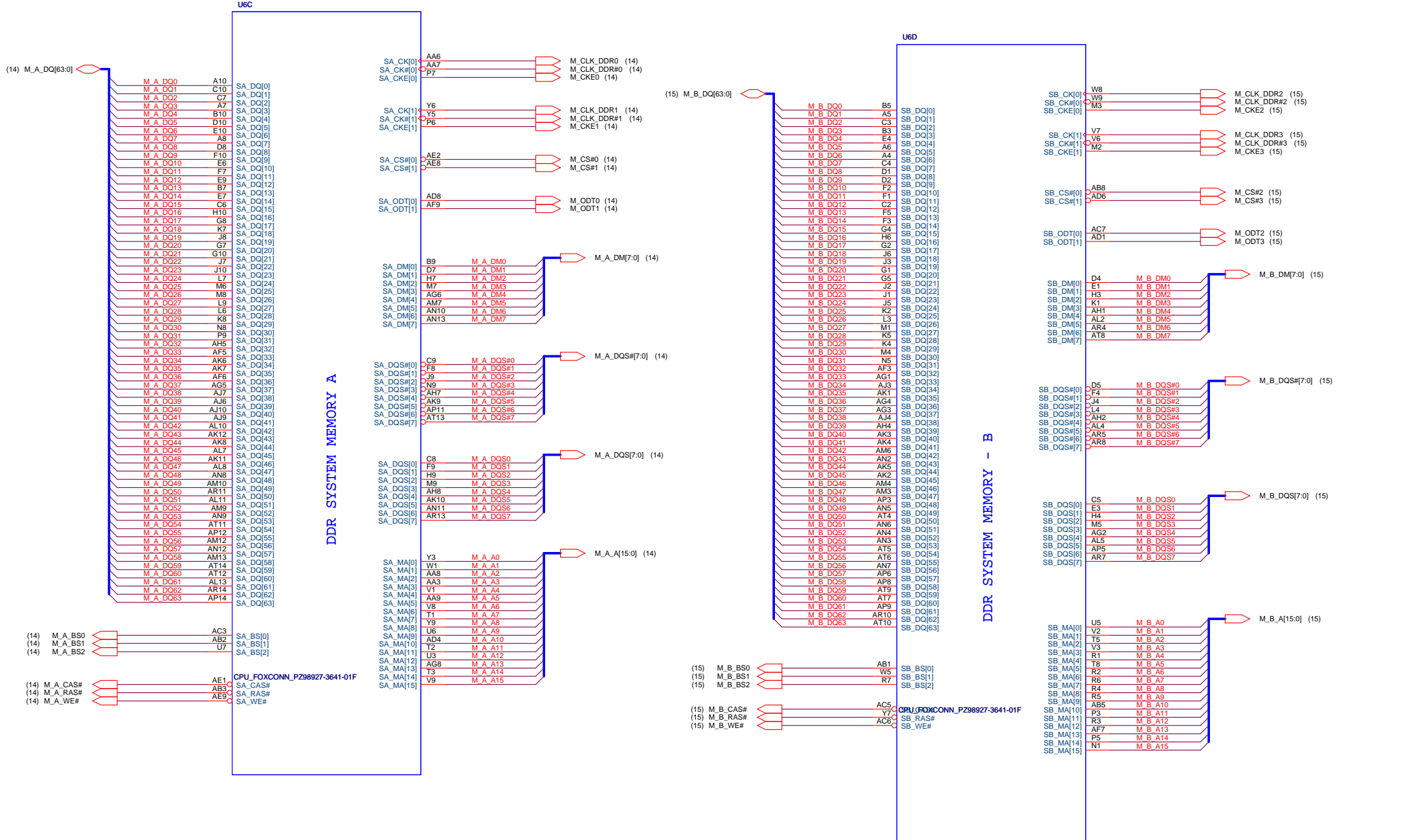
CPU\_FOXCONN\_PZ98927-3641-01F

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# ARRANDALE /CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

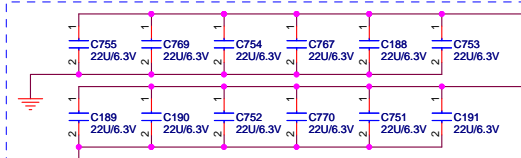


ARRANDALE /CLARKSFIELD PROCESSOR (DDR3)

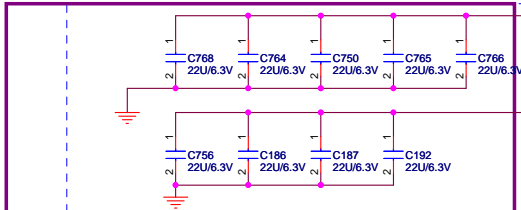




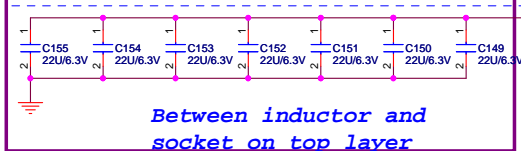
# ARRANDALE /CLARKSFIELD PROCESSOR (POWER)



Under cavity of the socket



Place inside cavity of the socket



Between inductor and  
socket on top layer

+VCC\_CORE

AG35 VCC1  
AG34 VCC2  
AG33 VCC3  
AG32 VCC4  
AG31 VCC5  
AG30 VCC6  
AG29 VCC7  
AG28 VCC8  
AG27 VCC9  
AG26 VCC10  
AF35 VCC11  
AF34 VCC12  
AF33 VCC13  
AF32 VCC14  
AF30 VCC15  
AF29 VCC16  
AF28 VCC17  
AF27 VCC18  
AF26 VCC19  
AD35 VCC20  
AD34 VCC21  
AD33 VCC22  
AD32 VCC23  
AD31 VCC24  
AD30 VCC25  
AD29 VCC26  
AD28 VCC27  
AD27 VCC28  
AD26 VCC29  
AC35 VCC30  
AC34 VCC31  
AC33 VCC32  
AC32 VCC33  
AC31 VCC34  
AC30 VCC35  
AC29 VCC36  
AC28 VCC37  
AC27 VCC38  
AC26 VCC39  
AA35 VCC40  
AA34 VCC41  
AA33 VCC42  
AA32 VCC43  
AA31 VCC44  
AA30 VCC45  
AA29 VCC46  
AA28 VCC47  
AA27 VCC48  
AA26 VCC49  
Y35 VCC50  
Y34 VCC51  
Y33 VCC52  
Y32 VCC53  
Y31 VCC54  
Y30 VCC55  
Y29 VCC56  
Y28 VCC57  
Y27 VCC58  
Y26 VCC59  
Y25 VCC60  
Y24 VCC61  
Y23 VCC62  
Y22 VCC63  
Y21 VCC64  
Y20 VCC65  
Y19 VCC66  
Y18 VCC67  
Y17 VCC68  
Y16 VCC69  
Y15 VCC70  
Y14 VCC71  
Y13 VCC72  
Y12 VCC73  
Y11 VCC74  
Y10 VCC75  
Y09 VCC76  
Y08 VCC77  
Y07 VCC78  
Y06 VCC79  
Y05 VCC80  
Y04 VCC81  
Y03 VCC82  
Y02 VCC83  
Y01 VCC84  
R35 VCC85  
R34 VCC86  
R33 VCC87  
R32 VCC88  
R31 VCC89  
R30 VCC90  
R29 VCC91  
R28 VCC92  
R27 VCC93  
R26 VCC94  
R25 VCC95  
R24 VCC96  
R23 VCC97  
R22 VCC98  
R21 VCC99  
R20 VCC100

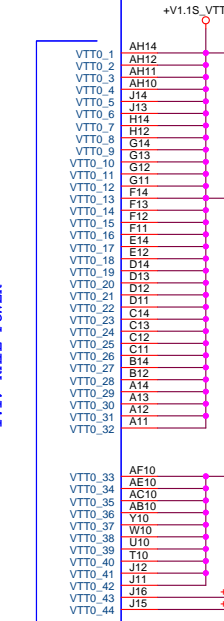
CPU CORE SUPPLY

1.1V RAIL POWER

POWER

CPU VIDS

SENSE LINES



+V1.1S\_VTT

+V1.1S\_VTT\_P

Edge of the socket

EMI

Under cavity of the socket

+V1.1S\_VTT33\_VTT42

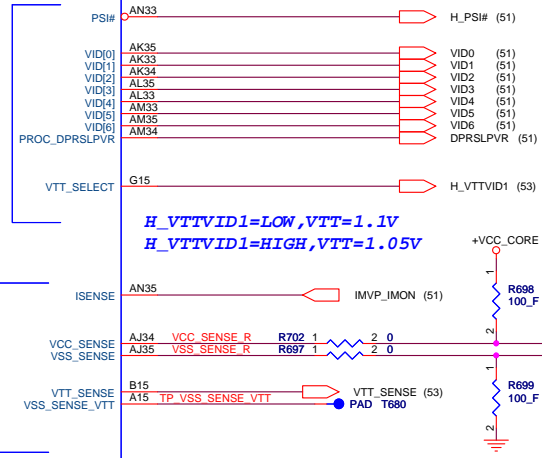
+V1.1S\_VTT

CRB min width:  
64 mils

+VTT\_43  
+VTT\_44

+V1.1S\_VTT

0402-SHORT



H\_VTTVID1=LOW,VTT=1.1V  
H\_VTTVID1=HIGH,VTT=1.05V

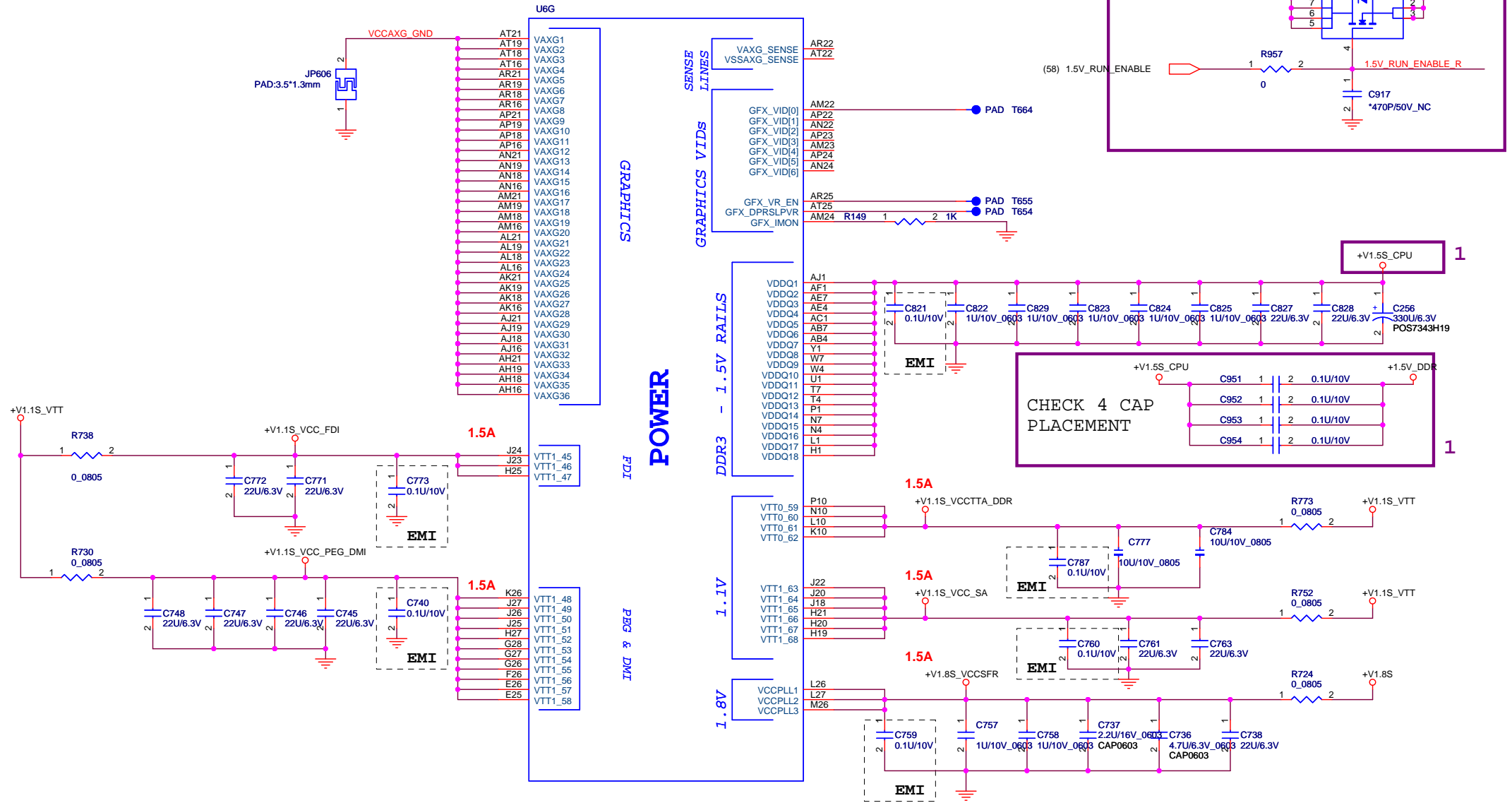
+VCC\_CORE

R698  
100\_F

R699  
100\_F

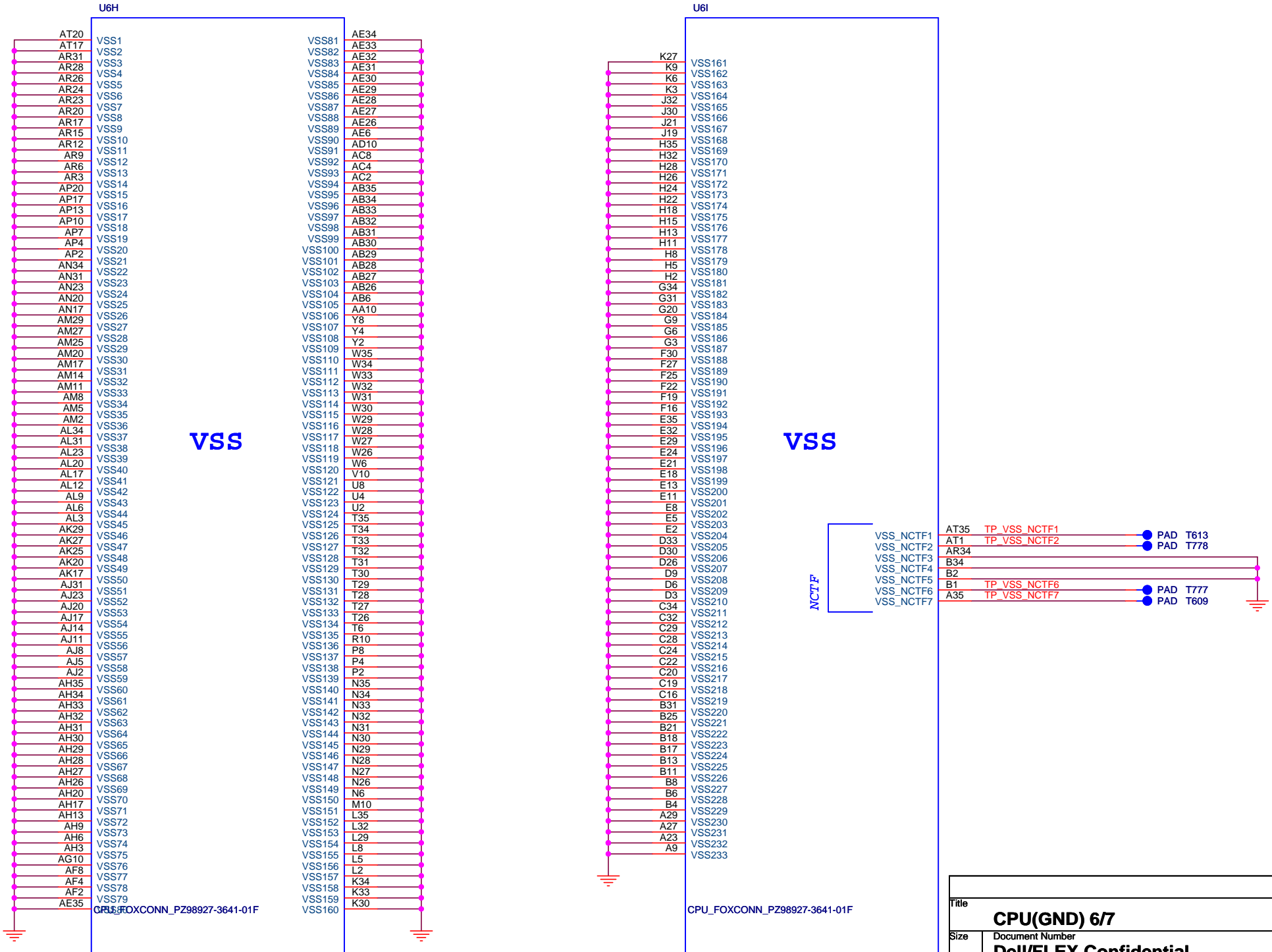
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# ARRANDALE /CLARKSFIELD PROCESSOR (GRAPHICS POWER)

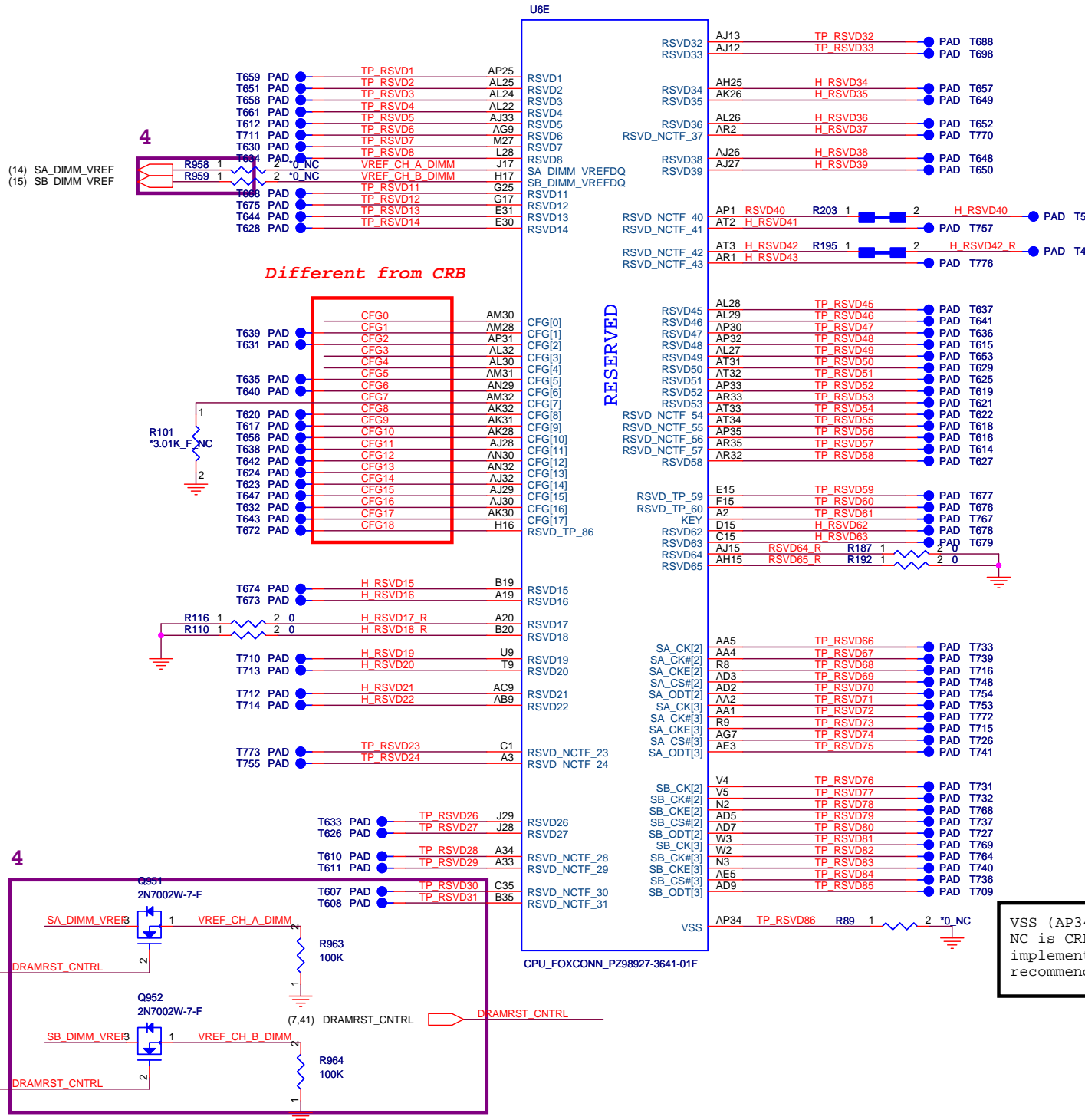


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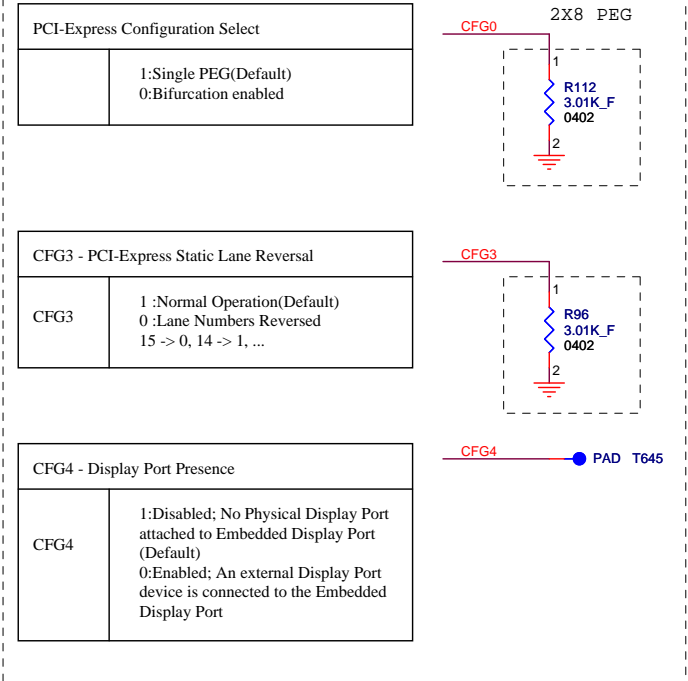
ARRANDALE /CLARKSFIELD PROCESSOR (GND)



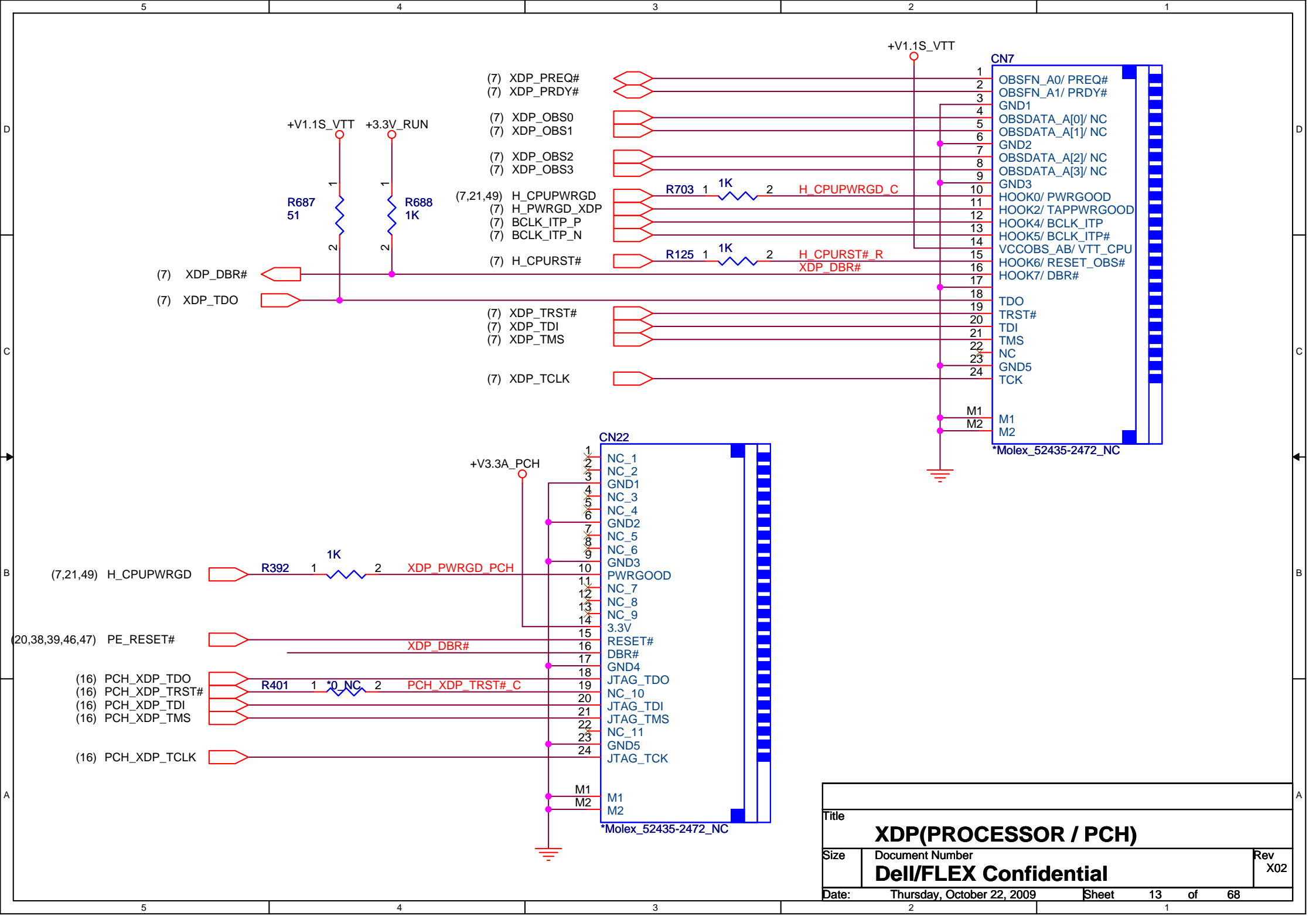
# ARRANDALE /CLARKSFIELD PROCESSOR( RESERVED, CFG)

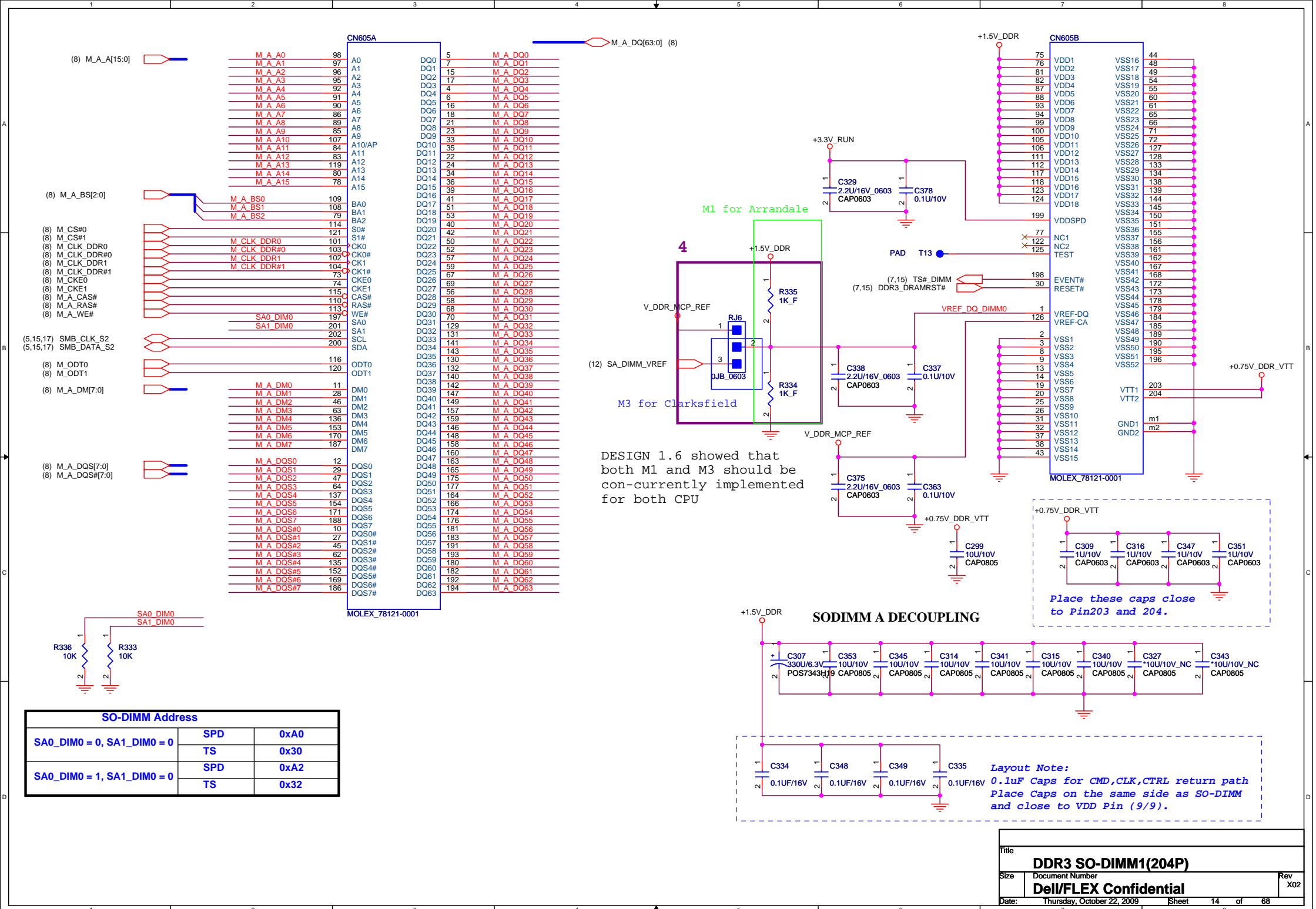


## CFG Straps for PROCESSOR



VSS (AP34) can be left  
NC is CRB  
implementation; EDS/DG  
recommendation to GND





(8) M\_B\_A[15:0]

(8) M\_B\_BS[2:0]

(8) M\_CS#2  
(8) M\_CS#3  
(8) M\_CLK\_DDR2  
(8) M\_CLK\_DDR#2  
(8) M\_CLK\_DDR3  
(8) M\_CLK\_DDR#3  
(8) M\_CKE2  
(8) M\_CKE3  
(8) M\_B\_CAS#  
(8) M\_B\_RAS#  
(8) M\_B\_WE#

(5,14,17) SMB\_CLK\_S2  
(5,14,17) SMB\_DATA\_S2

(8) M\_ODT2  
(8) M\_ODT3

(8) M\_B\_DM[7:0]

(8) M\_B\_DQS[7:0]  
(8) M\_B\_DQS#7:0

+3.3V\_RUN

R360  
10K

SA1\_DIM1

R369  
10K

SA0\_DIM1

#### SO-DIMM Address

SPD	0xA4
TS	0x34

M\_B\_A0 98  
M\_B\_A1 97  
M\_B\_A2 96  
M\_B\_A3 95  
M\_B\_A4 92  
M\_B\_A5 91  
M\_B\_A6 90  
M\_B\_A7 89  
M\_B\_A8 88  
M\_B\_A9 85  
M\_B\_A10 107  
M\_B\_A11 84  
M\_B\_A12 83  
M\_B\_A13 119  
M\_B\_A14 80  
M\_B\_A15 78

M\_B\_BS0 109  
M\_B\_BS1 108  
M\_B\_BS2 79

M\_CLK\_DDR2 101  
M\_CLK\_DDR#2 103  
M\_CLK\_DDR3 102  
M\_CLK\_DDR#3 104

SA0\_DIM1 197  
SA1\_DIM1 201

SCL 202  
SDA 200

ODT0 116  
ODT1 120

M\_B\_DM0 11  
M\_B\_DM1 28  
M\_B\_DM2 46  
M\_B\_DM3 63  
M\_B\_DM4 136  
M\_B\_DM5 153  
M\_B\_DM6 170  
M\_B\_DM7 187

M\_B\_DQS0 12  
M\_B\_DQS1 29  
M\_B\_DQS2 47  
M\_B\_DQS3 64  
M\_B\_DQS4 137  
M\_B\_DQS5 154  
M\_B\_DQS6 171  
M\_B\_DQS7 188  
M\_B\_DQS#0 10  
M\_B\_DQS#1 27  
M\_B\_DQS#2 45  
M\_B\_DQS#3 62  
M\_B\_DQS#4 135  
M\_B\_DQS#5 152  
M\_B\_DQS#6 169  
M\_B\_DQS#7 186

MOLEX\_78192-0001

CN606A

A0 5  
A1 7  
A2 15  
A3 17  
A4 4  
A5 6  
A6 16  
A7 18  
A8 21  
A9 23  
A10/AP 33  
A11 35  
A12 22  
A13 24  
A14 34  
A15 36

BA0 109  
BA1 108  
BA2 79  
S0# 114  
S1# 121  
CK0 101  
CK0# 103  
CK1 102  
CK1# 104  
CKE0 73  
CKE1 74  
CAS# 115  
RAS# 113  
WE# 119  
SA0 201  
SA1 202  
SDA 200

ODT0 116  
ODT1 120

DM0 11  
DM1 28  
DM2 46  
DM3 63  
DM4 136  
DM5 153  
DM6 170  
DM7 187

DQS0 12  
DQS1 29  
DQS2 47  
DQS3 64  
DQS4 137  
DQS5 154  
DQS6 171  
DQS7 188  
DQS#0 10  
DQS#1 27  
DQS#2 45  
DQS#3 62  
DQS#4 135  
DQS#5 152  
DQS#6 169  
DQS#7 186

MOLEX\_78192-0001

CN606B

DQ0 5  
DQ1 7  
DQ2 15  
DQ3 17  
DQ4 4  
DQ5 6  
DQ6 16  
DQ7 18  
DQ8 21  
DQ9 23  
DQ10 33  
DQ11 35  
DQ12 22  
DQ13 24  
DQ14 34  
DQ15 36

DQ16 39  
DQ17 41  
DQ18 51  
DQ19 40  
DQ20 42  
DQ21 50  
DQ22 52  
DQ23 57  
DQ24 59  
DQ25 67  
DQ26 69  
DQ27 67  
DQ28 58  
DQ29 68  
DQ30 70  
DQ31 129  
DQ32 131  
DQ33 141  
DQ34 143  
DQ35 130  
DQ36 132  
DQ37 140  
DQ38 142  
DQ39 147  
DQ40 149  
DQ41 157  
DQ42 159  
DQ43 146  
DQ44 148  
DQ45 158  
DQ46 160  
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DQ55 181  
DQ56 183  
DQ57 191  
DQ58 193  
DQ59 180  
DQ60 182  
DQ61 192  
DQ62 194  
DQ63 194

DM0 11  
DM1 28  
DM2 46  
DM3 63  
DM4 136  
DM5 153  
DM6 170  
DM7 187

DQS0 12  
DQS1 29  
DQS2 47  
DQS3 64  
DQS4 137  
DQS5 154  
DQS6 171  
DQS7 188  
DQS#0 10  
DQS#1 27  
DQS#2 45  
DQS#3 62  
DQS#4 135  
DQS#5 152  
DQS#6 169  
DQS#7 186

DQS0 12  
DQS1 29  
DQS2 47  
DQS3 64  
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DQS6 171  
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DQS#3 62  
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DQS#5 152  
DQS#6 169  
DQS#7 186

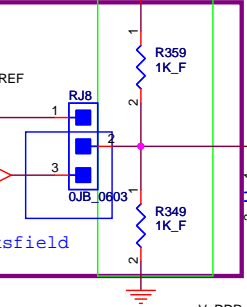
(12) SB\_DIMM\_VREF

M3 for Clarkfield

DESIGN 1.6 showed that both M1 and M3 should be con-currently implemented for both CPU

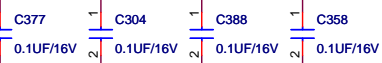
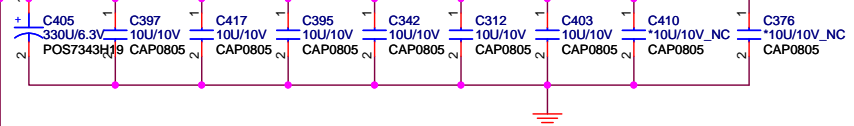
M1 for Arrandale

4



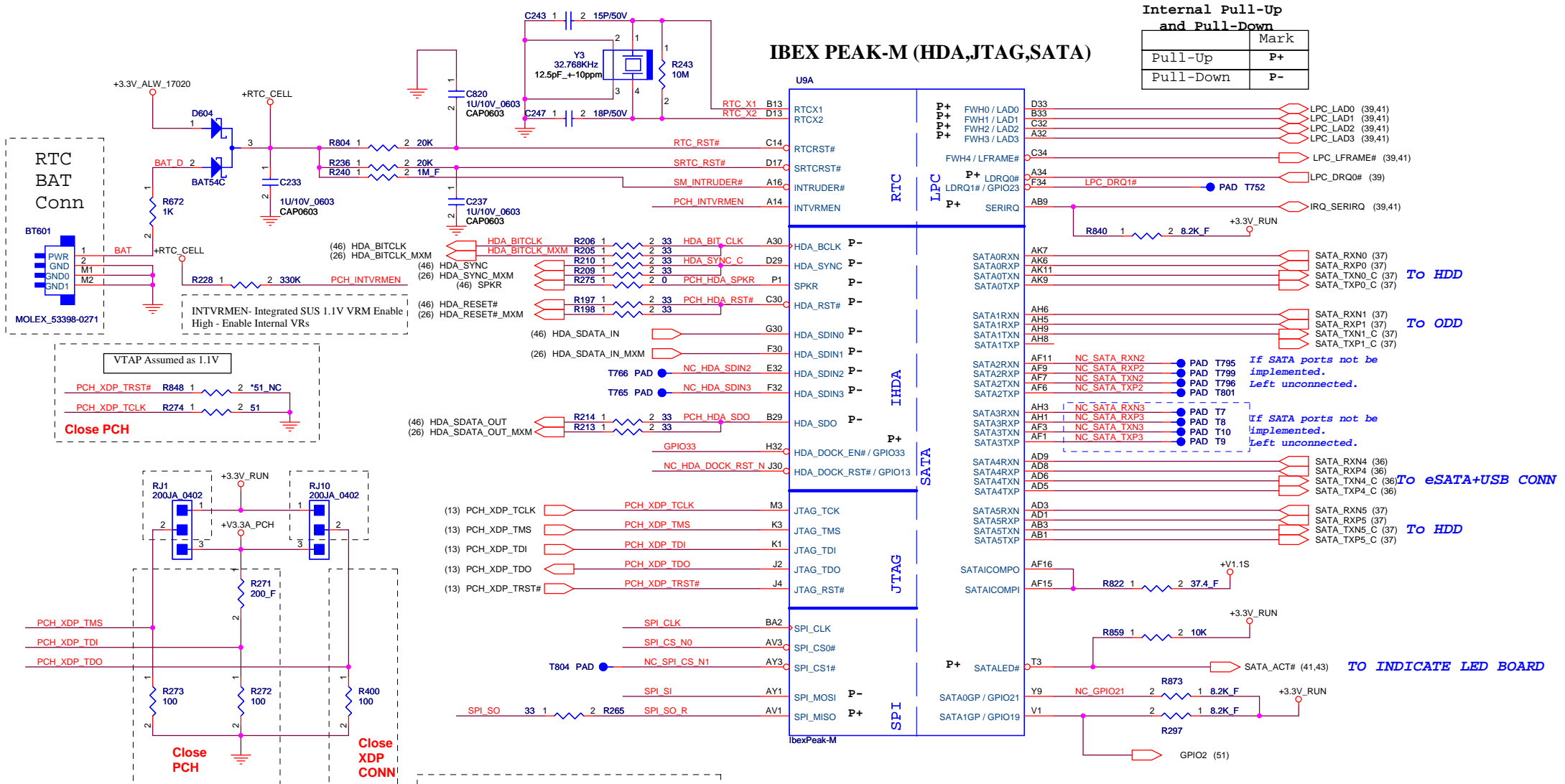
+1.5V\_DDR

#### SODIMM 2 DECOUPLING



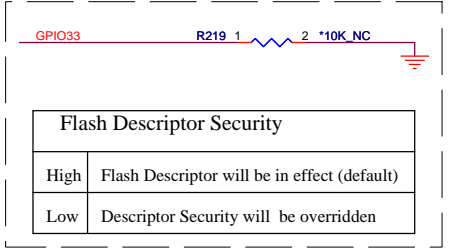
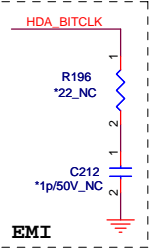
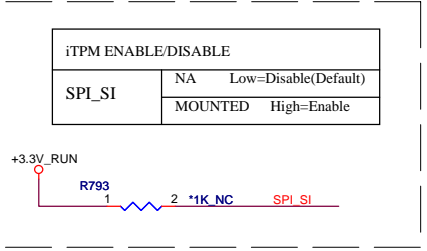
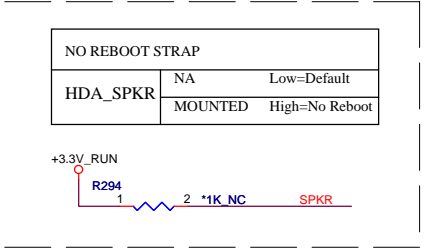
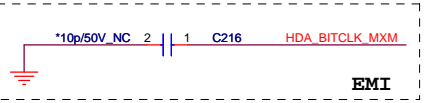
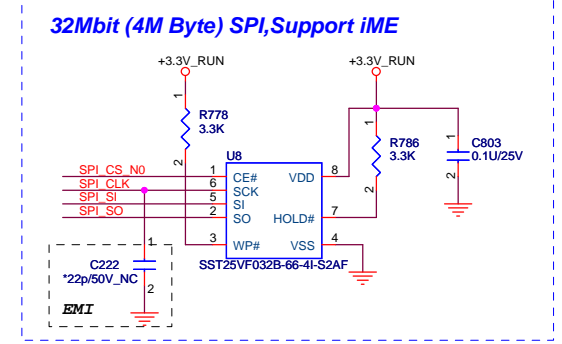
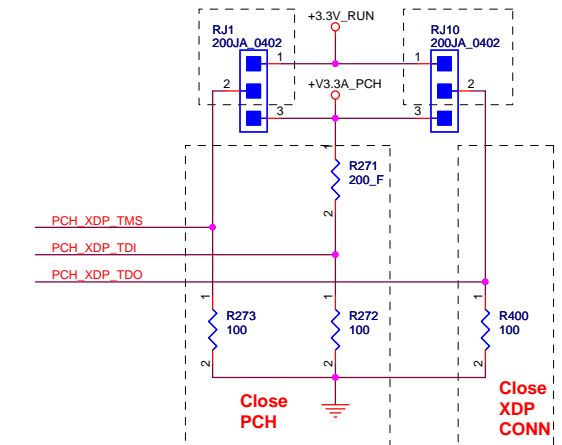
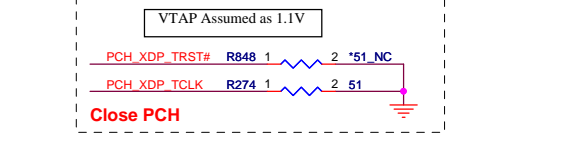
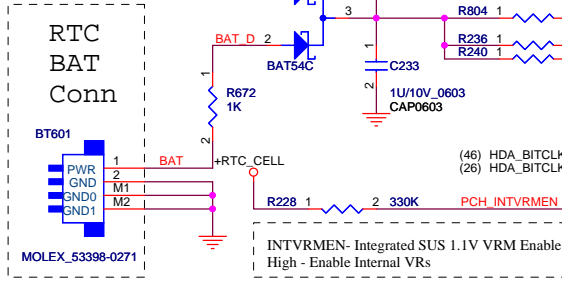
Layout Note:  
0.1uF Caps for CMD,CLK,CTRL return path  
Place Caps on the same side as SO-DIMM  
and close to VDD Pin (9/9).





Internal Pull-Up and Pull-Down

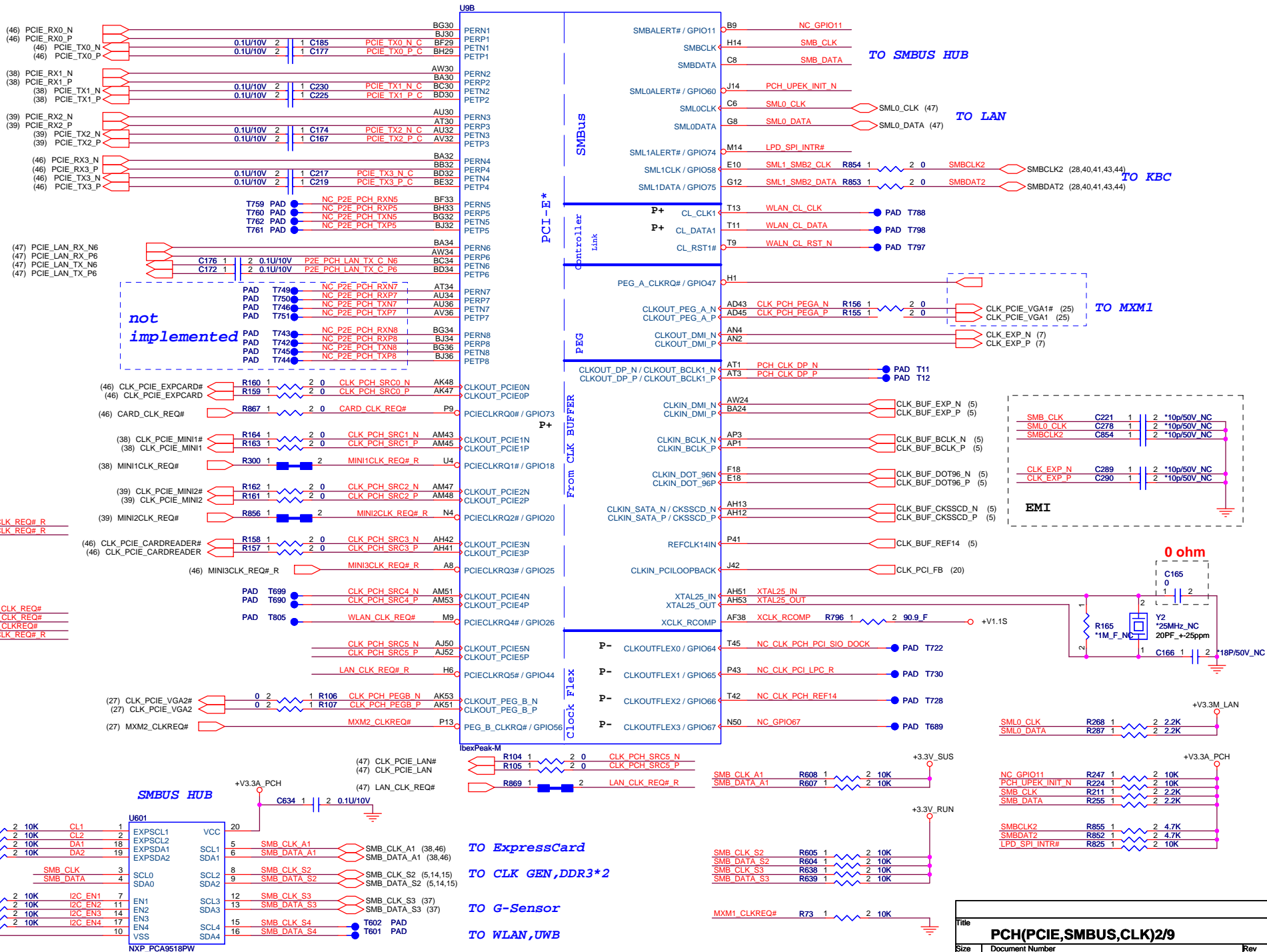
	Mark
Pull-Up	P+
Pull-Down	P-



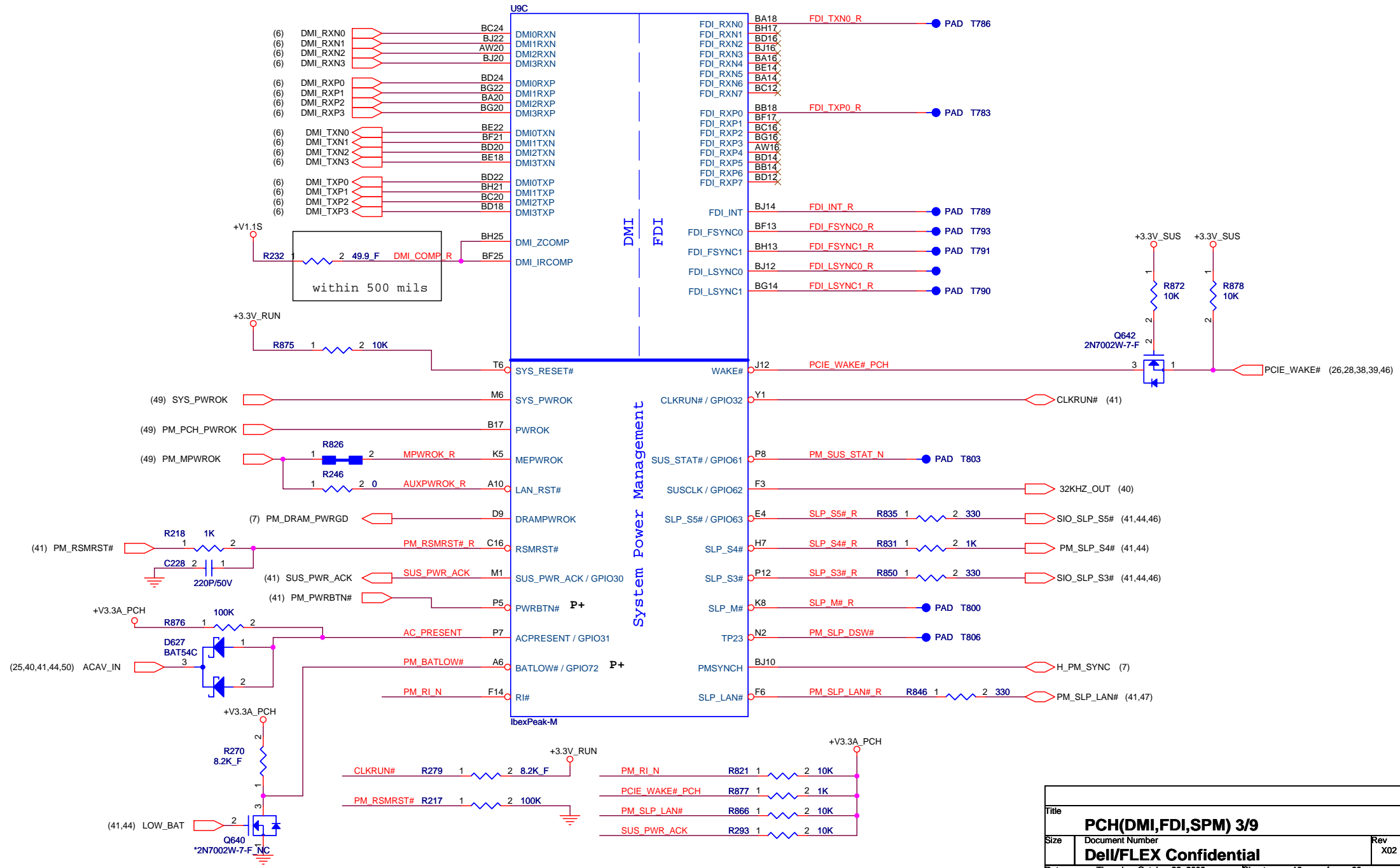


# IBEX PEAK-M (PCI-E,SMBUS,CLK)

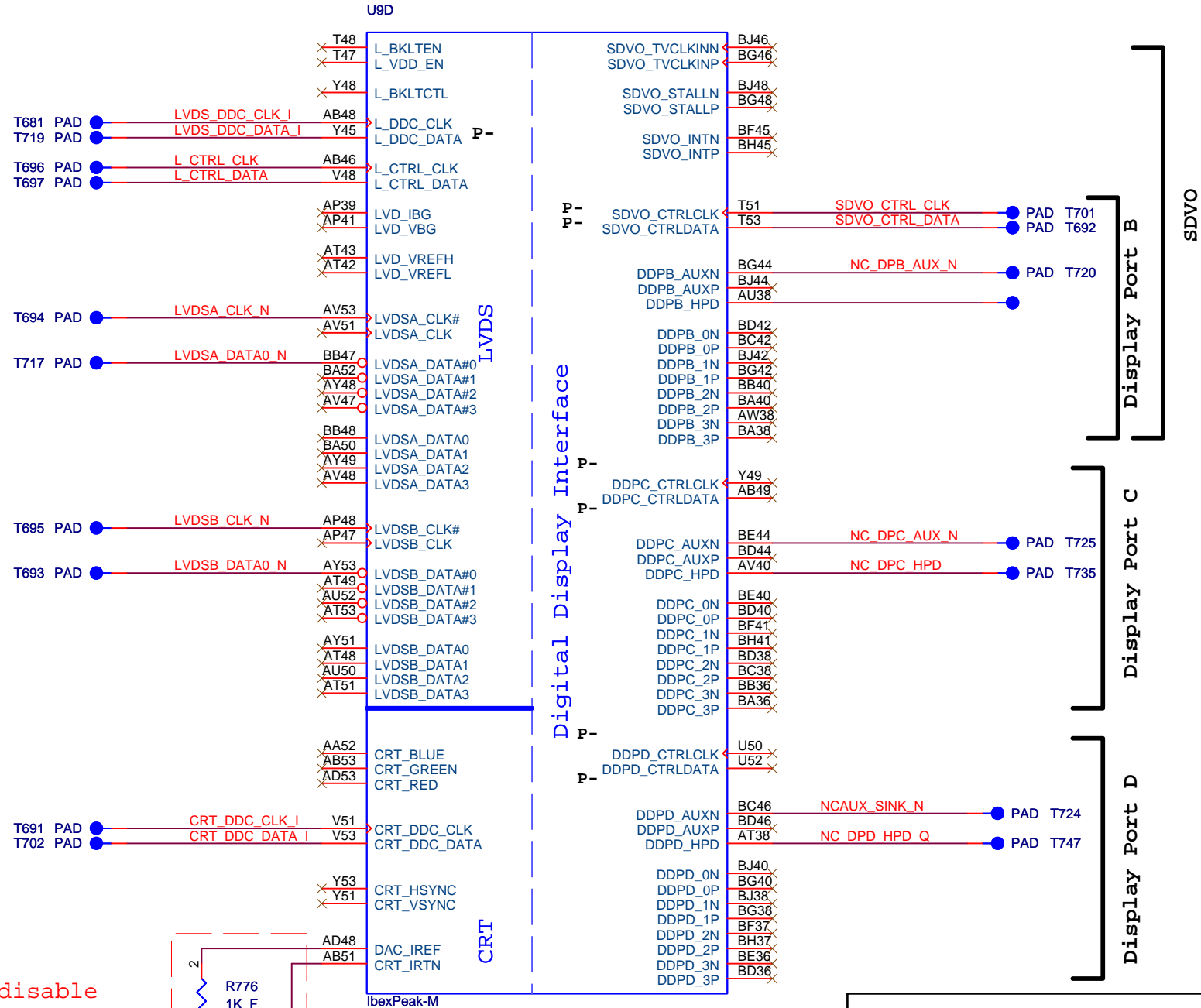
PCI-E* x1	Usage
Lane 1	Express Card
Lane2	WiMax
Lane 3	BT
Lane 4	Card reader/1394
Lane 5	NC
Lane 6	PHY
Lane 7	NC
Lane 8	NC

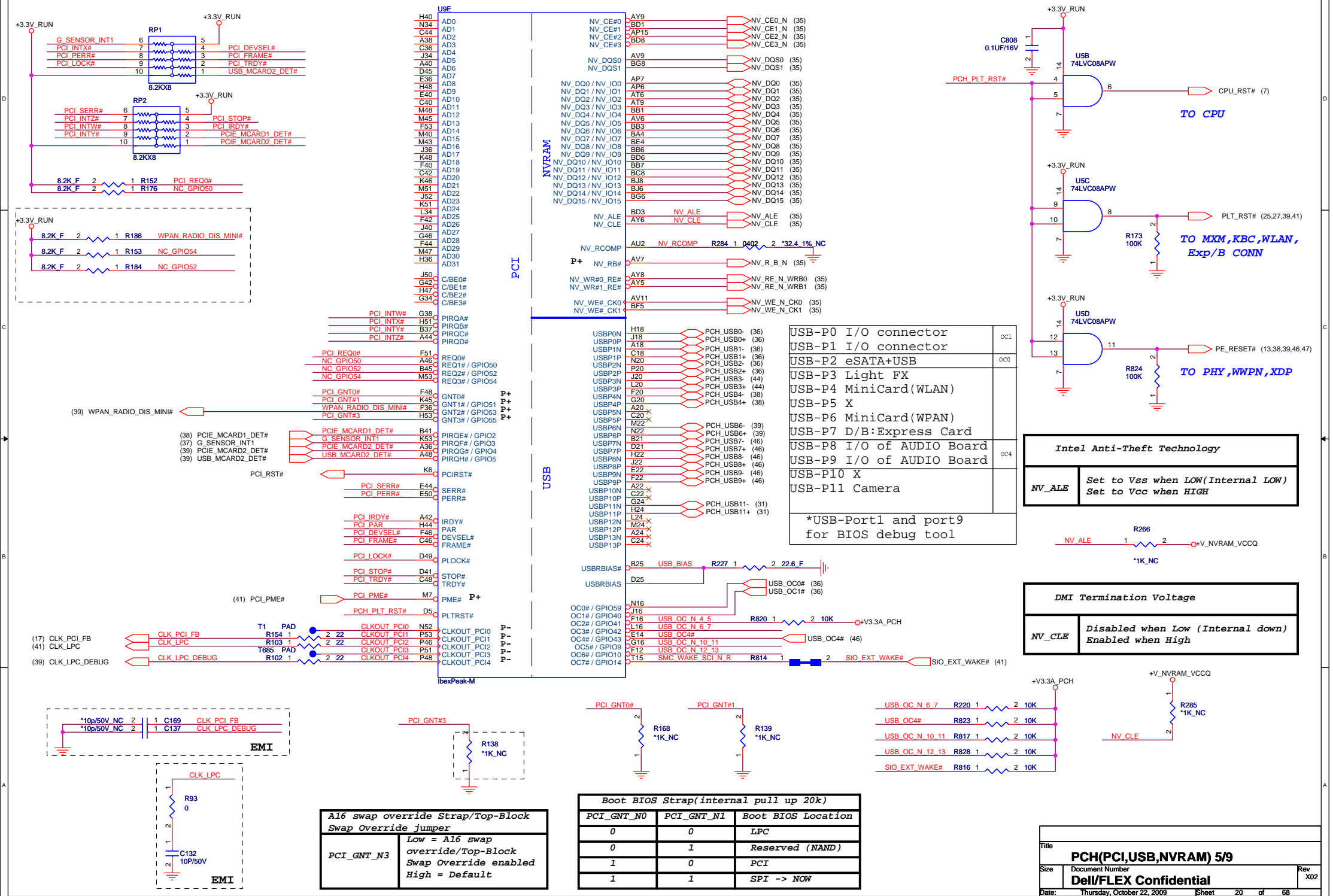


# IBEX PEAK-M (DMI,FDI,GPIO)

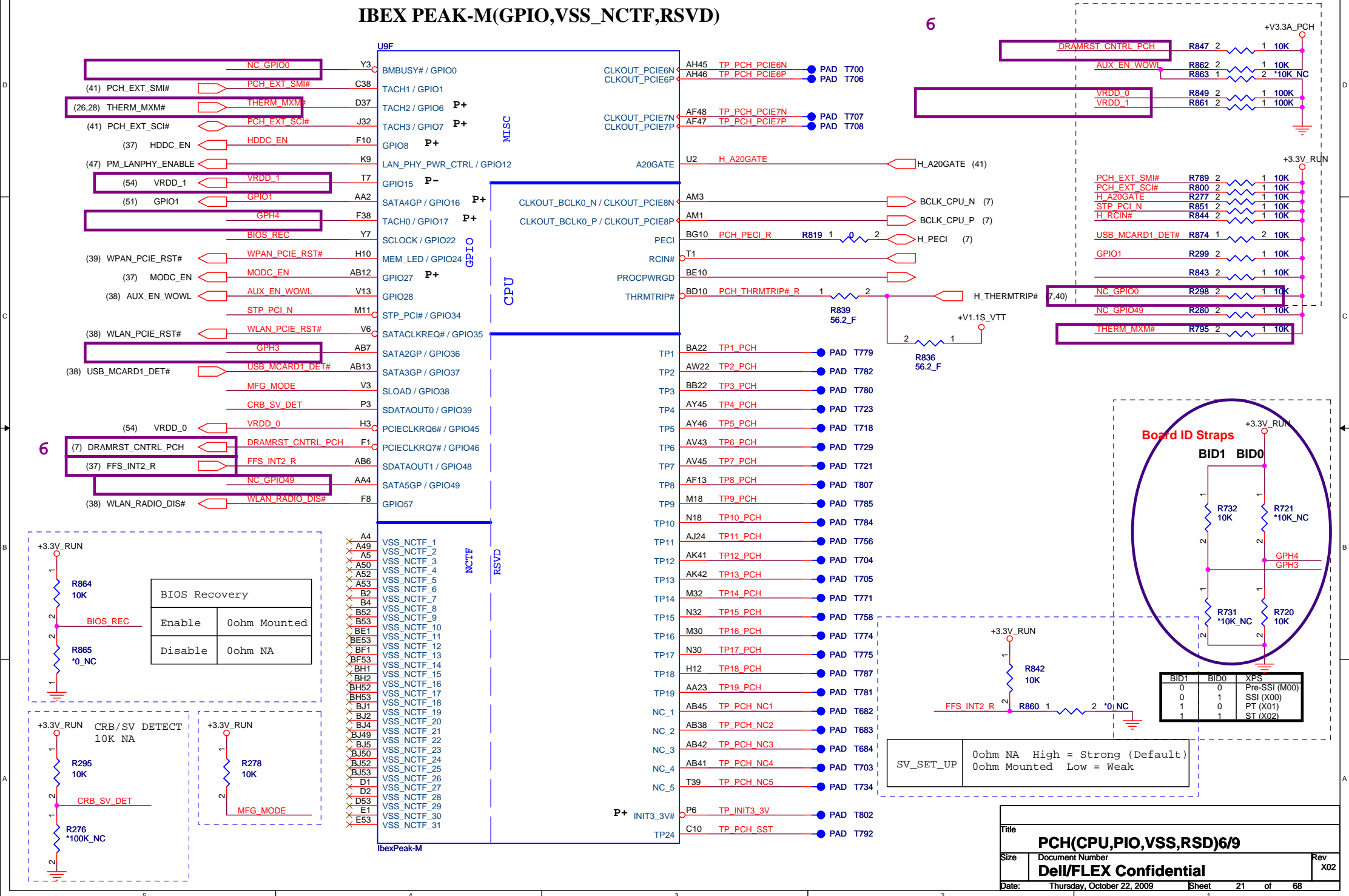


# IBEX PEAK-M (LVDS,DDI)



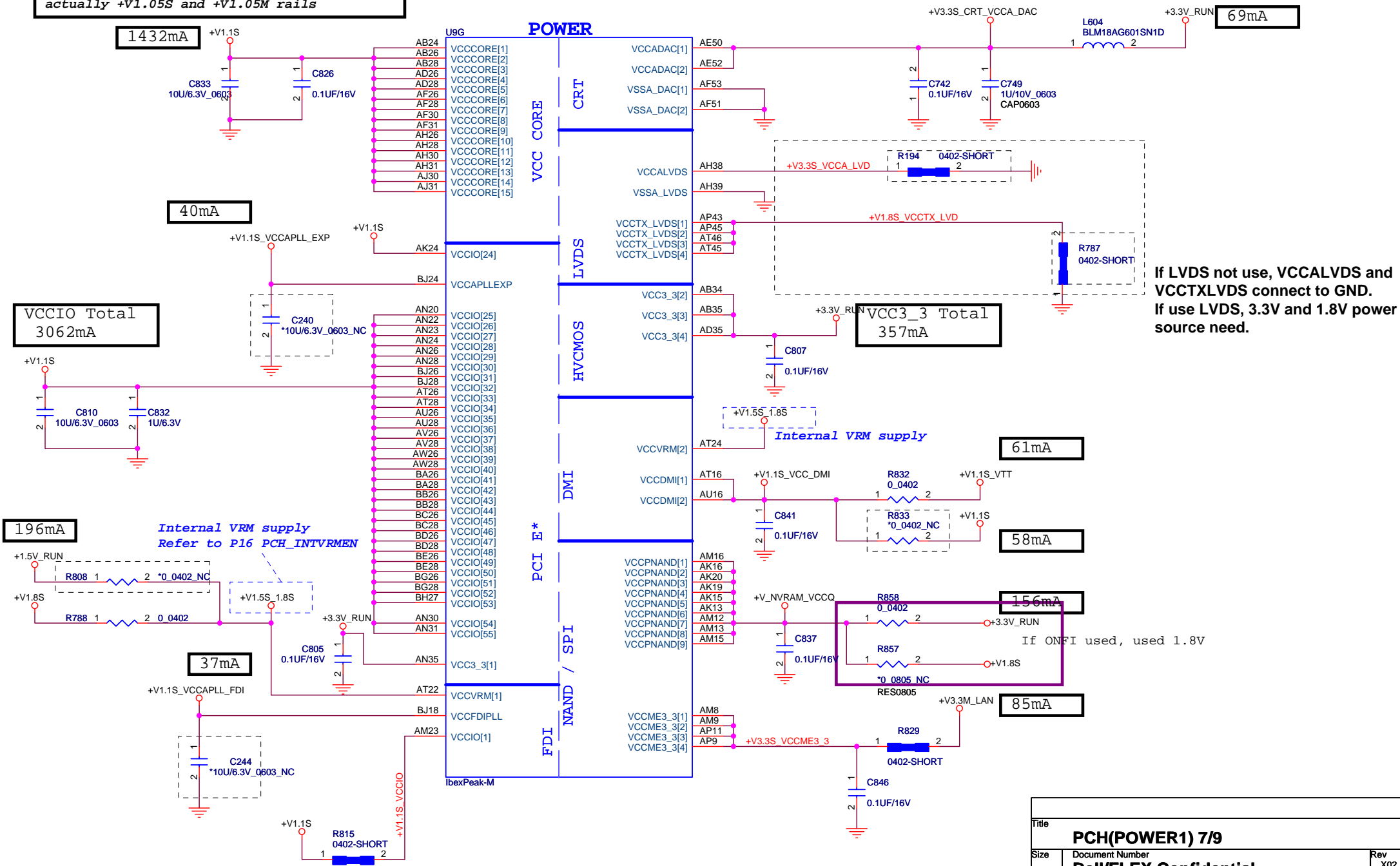
**IBEX PEAK-M (PCI,USB,INTEL(R) TURBO MEMORY)**

## IBEX PEAK-M(GPIO,VSS\_NCTF,RSVD)



Please note that all Ibex Peak-M rails with netnames +V1.1S and +V1.1M rails are actually +V1.05S and +V1.05M rails

## IBEX PEAK-M(POWER)





# IBEX PEAK-M(POWER)

## POWER

## USB

## Clock and Miscellaneous

## PCI/GPIO/LPC

## PCI/GPIO/LPC

## CPU

## RTC

## HDA

VCCIO Total  
3062mA

VCCSUS3\_3 Total  
163mA

VCC3\_3 Total  
357mA

31mA

6mA

VCCME Total  
3062mA

1UF\*2 pcs  
for 2 blocks

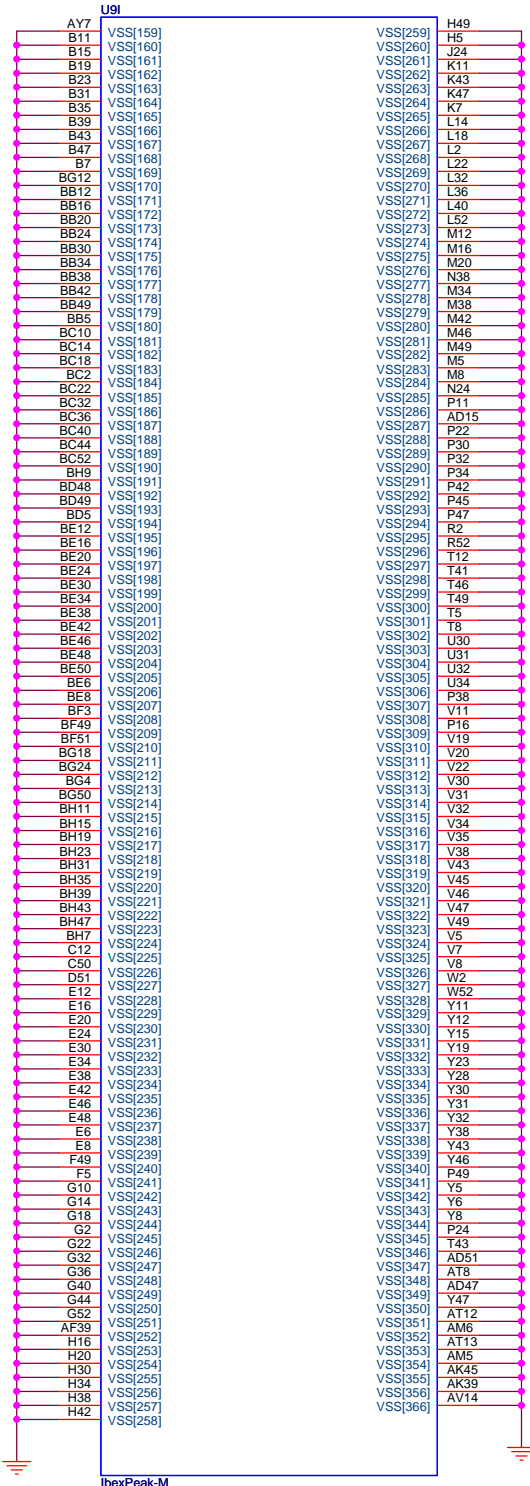
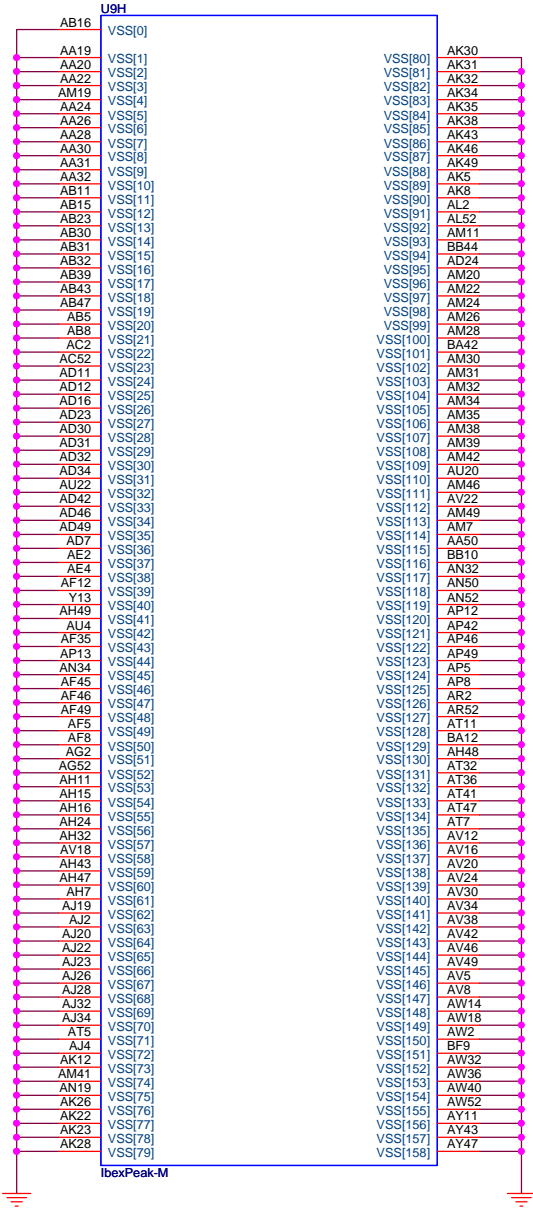
Internal VRM supply

Internal VRM supply

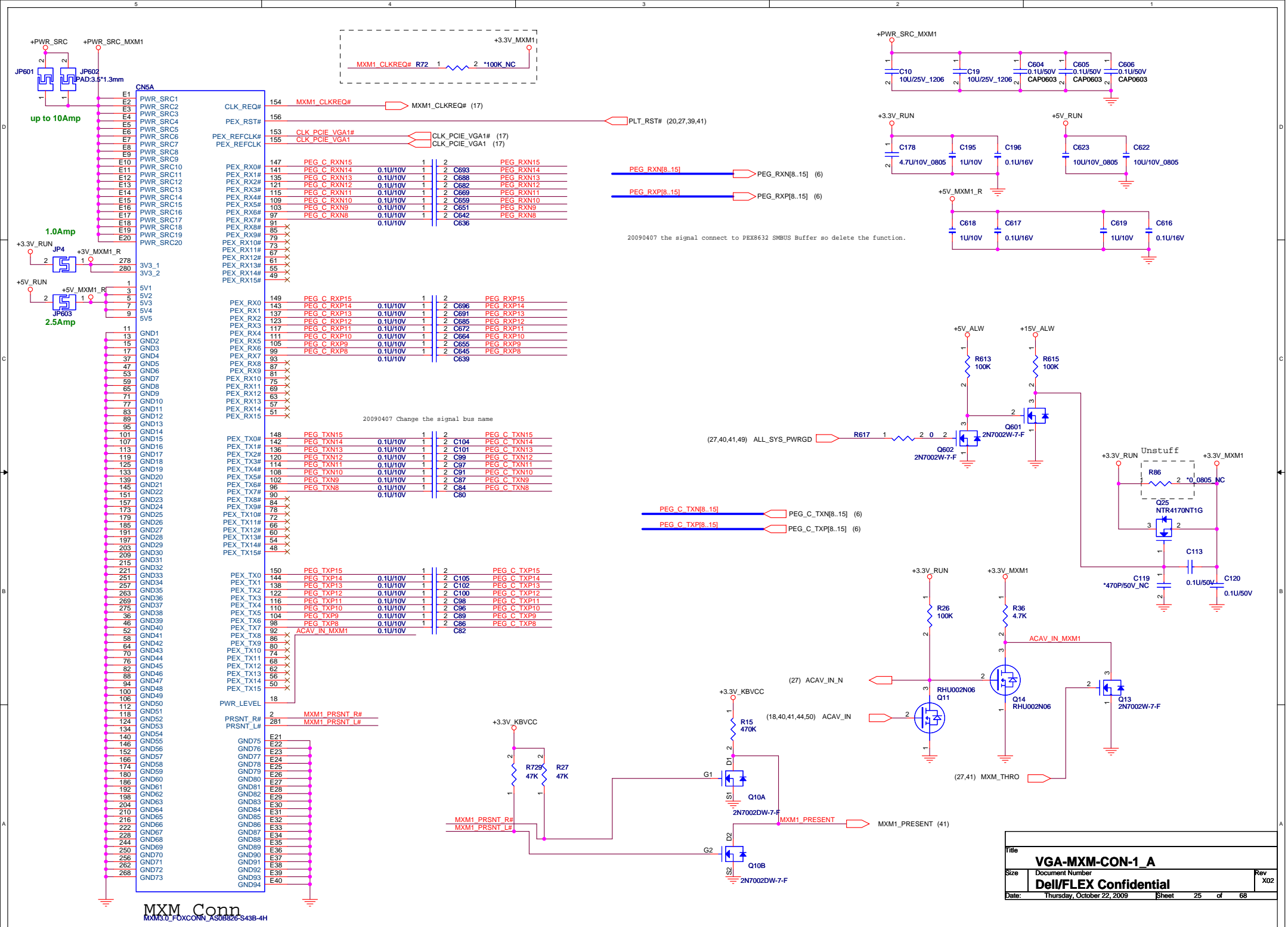
+5V\_ALW has off during  
S4/S5 battery mode.

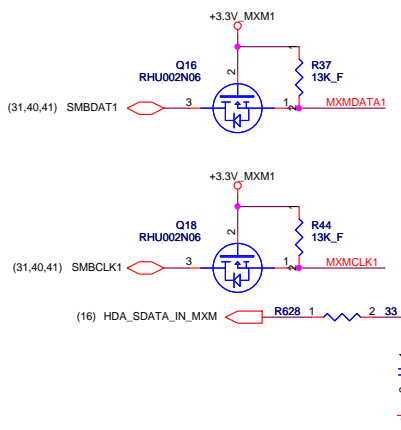
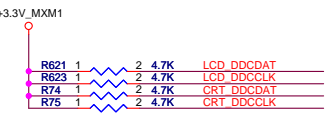
Please note that all Ibex Peak-M  
rails with netnames +V1.1S and  
+V1.1M rails are actually +V1.05S  
and +V1.05M rails

IBEX PEAK-M (GND)



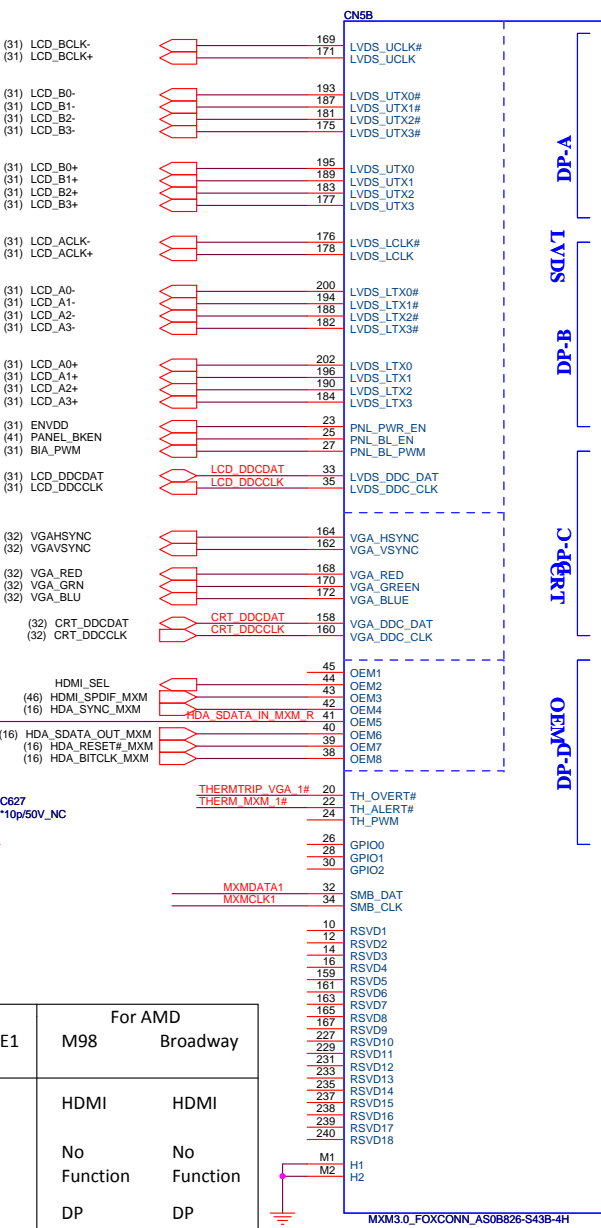




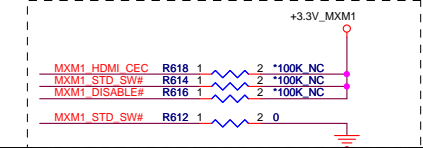
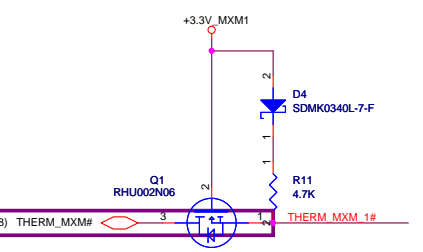
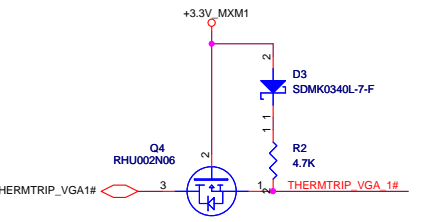
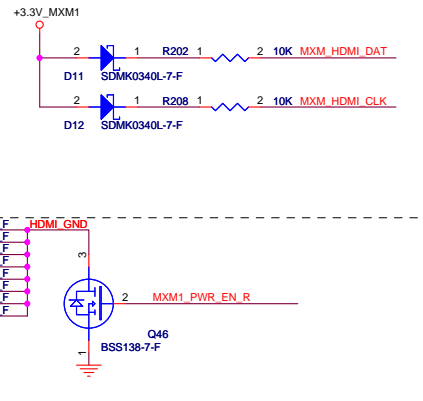
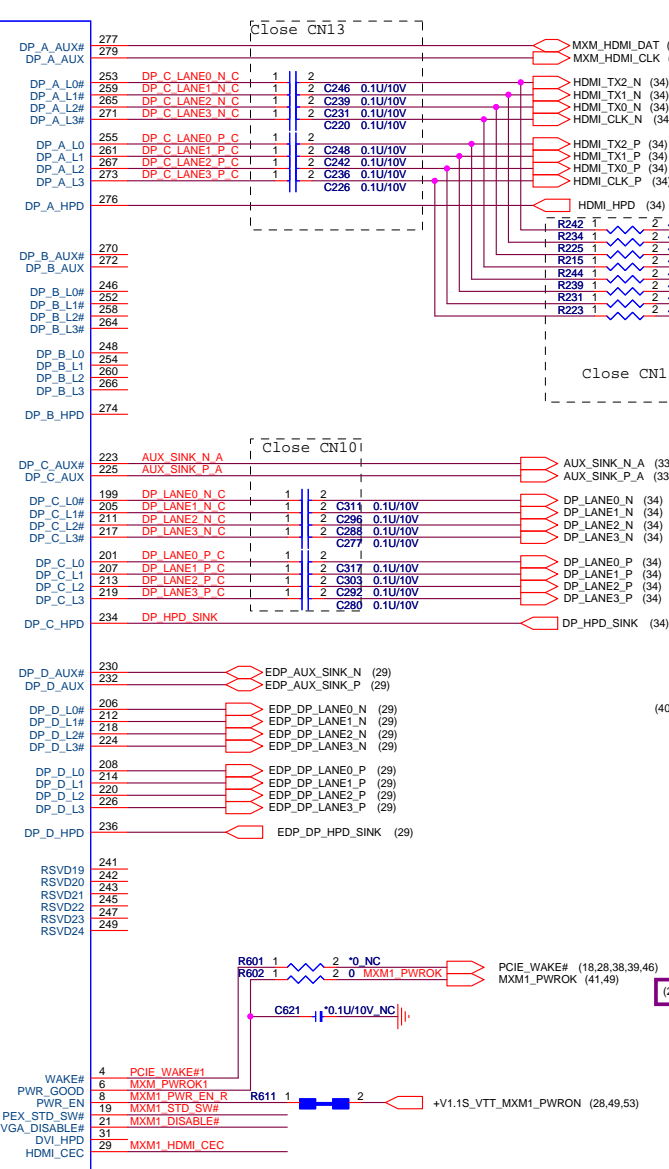


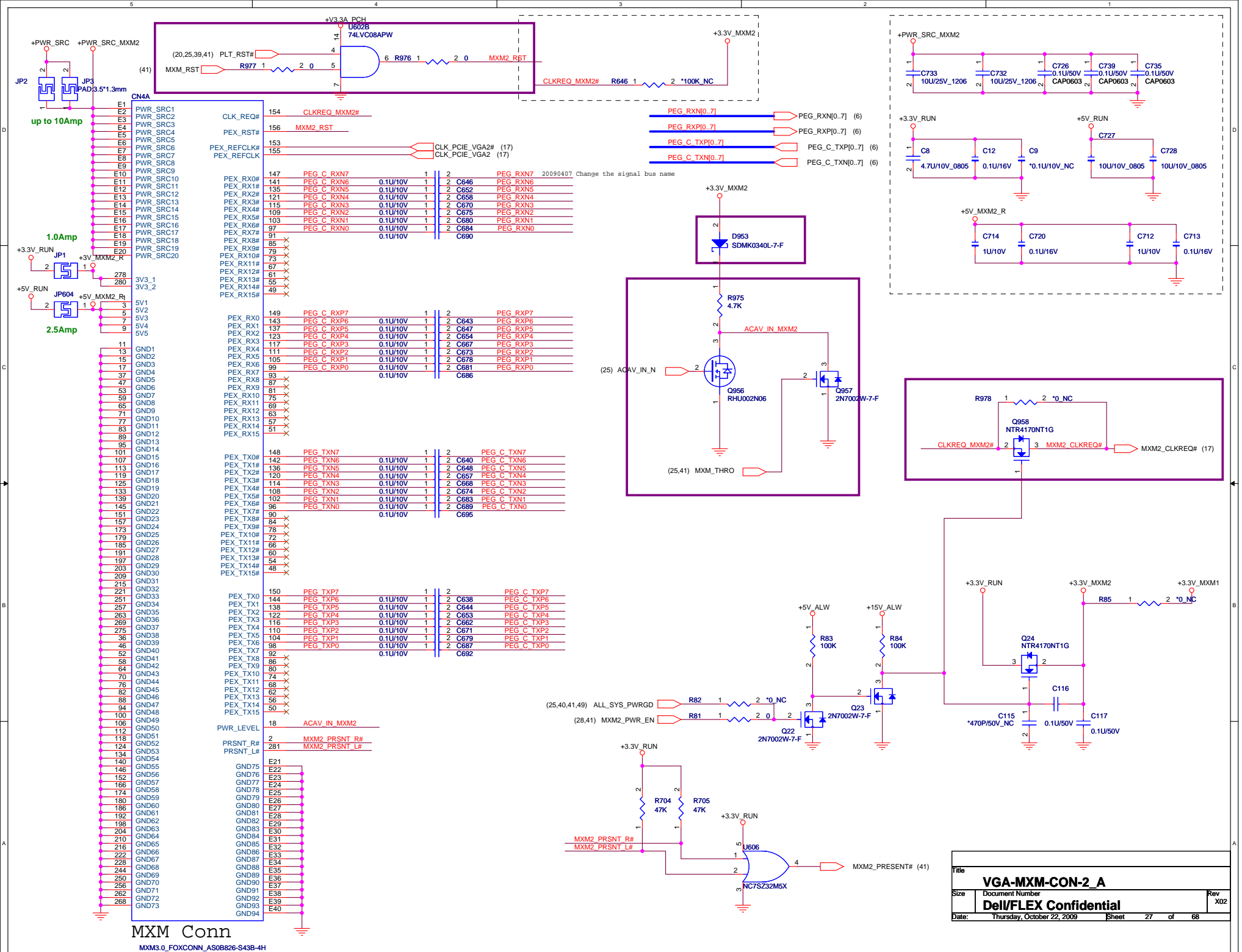
MLK Define	For NV			For AMD	
	N10E-GTX1	N11E-GTX1	N11E-GS1/GE1	M98	Broadway
DPA	HDMI *	HDMI	HDMI	HDMI	HDMI
DPB	No Function	No Function	No Function	No Function	No Function
DPC	No Function	DP *	DP	DP	DP
DPD	No Function	eDP *	eDP	No Function	eDP

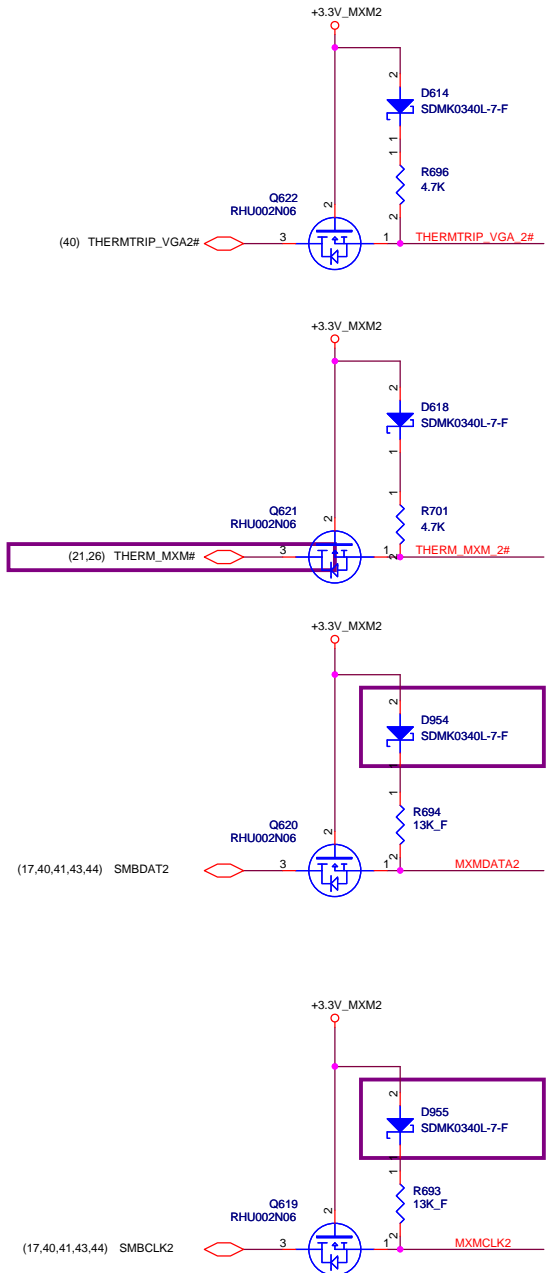
Note: N10E-GTX1 HDMI output by S/W programming.  
N11E-GTX1 DP/eDP can't support clone mode.



MXM Conn

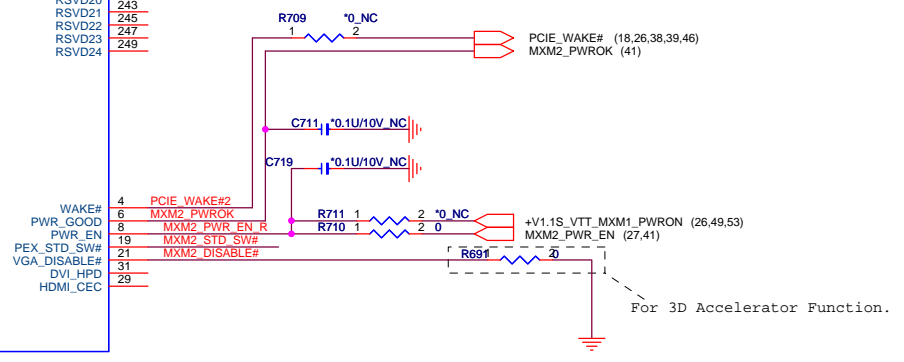
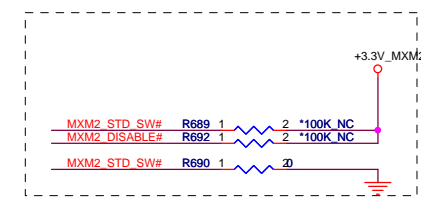






CN4B		CN4B	
169	LVDS_UCLK#	277	DP_A_AUX#
171	LVDS_UCLK	279	DP_A_AUX
193	LVDS_UTX0#	253	DP_A_L0#
187	LVDS_UTX1#	259	DP_A_L1#
181	LVDS_UTX2#	265	DP_A_L2#
175	LVDS_UTX3#	271	DP_A_L3#
195	LVDS_UTX0	255	DP_A_L0
189	LVDS_UTX1	261	DP_A_L1
183	LVDS_UTX2	267	DP_A_L2
177	LVDS_UTX3	273	DP_A_L3
176	LVDS_LCLK#	276	DP_A_HPD
178	LVDS_LCLK	270	DP_B_AUX#
200	LVDS_LTX0#	272	DP_B_AUX
194	LVDS_LTX1#	246	DP_B_L0#
188	LVDS_LTX2#	252	DP_B_L1#
182	LVDS_LTX3#	258	DP_B_L2#
202	LVDS_LTX0	264	DP_B_L3#
196	LVDS_LTX1	248	DP_B_L0
190	LVDS_LTX2	254	DP_B_L1
184	LVDS_LTX3	260	DP_B_L2
23	PNL_PWR_EN	266	DP_B_L3
25	PNL_BL_EN	274	DP_B_HPD
27	PNL_BL_PWM	223	DP_C_AUX#
33	LVDS_DDC_DAT	225	DP_C_AUX
35	LVDS_DDC_CLK	199	DP_C_L0#
164	VGA_HSYNC	205	DP_C_L1#
162	VGA_VSYNC	211	DP_C_L2#
168	VGA_RED	217	DP_C_L3#
170	VGA_GREEN	201	DP_C_L0
172	VGA_BLUE	207	DP_C_L1
158	VGA_DDC_DAT	213	DP_C_L2
160	VGA_DDC_CLK	219	DP_C_L3
45	OEM1	234	DP_C_HPD
44	OEM2	230	DP_D_AUX#
43	OEM3	232	DP_D_AUX
42	OEM4	206	DP_D_L0#
41	OEM5	212	DP_D_L1#
40	OEM6	218	DP_D_L2#
39	OEM7	224	DP_D_L3#
38	OEM8	208	DP_D_L0
20	TH_OVERT#	214	DP_D_L1
22	TH_ALERT#	220	DP_D_L2
24	TH_PWM	226	DP_D_L3
26	GPIO0	236	DP_D_HPD
28	GPIO1	241	RSVD19
30	GPIO2	242	RSVD20
32	SMB_DAT	243	RSVD21
34	SMB_CLK	245	RSVD22
10	RSVD1	247	RSVD23
12	RSVD2	249	RSVD24
14	RSVD3	4	WAKE#
16	RSVD4	6	PWR_GOOD
159	RSVD5	8	PWR_EN
161	RSVD6	19	PEX_STD_SW#
163	RSVD7	21	VGA_DISABLE#
165	RSVD8	31	DVI_HPD
167	RSVD9	29	HDMI_CEC
227	RSVD10		
229	RSVD11		
231	RSVD12		
233	RSVD13		
235	RSVD14		
237	RSVD15		
238	RSVD16		
239	RSVD17		
240	RSVD18		
M1	H1		
M2	H2		

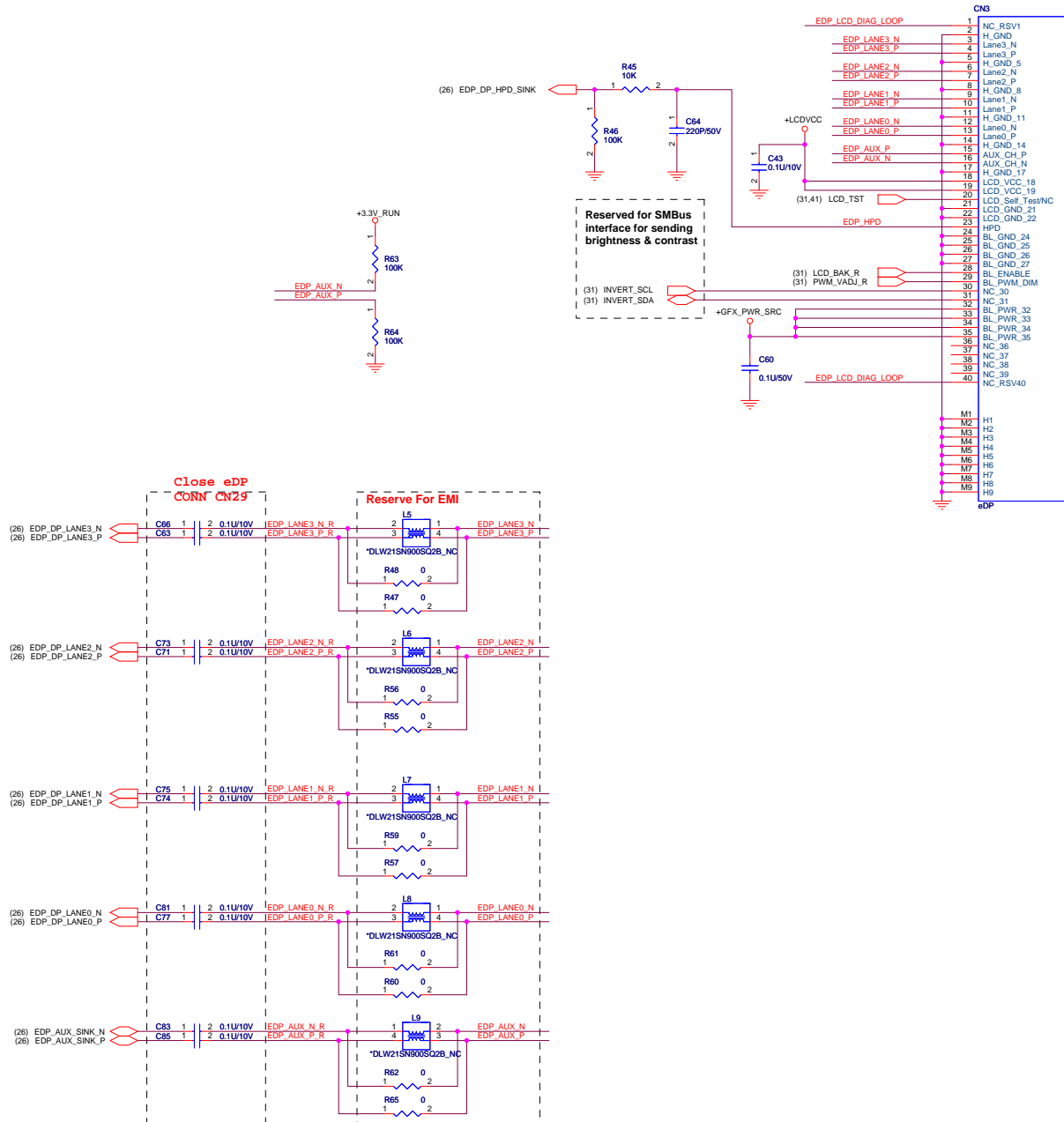
DP-A  
SDVI  
DP-B  
DP-C  
DP-D  
DP-E



MXM Conn

MXM3.0\_FOXCONN\_AS0B826-S43B-4H

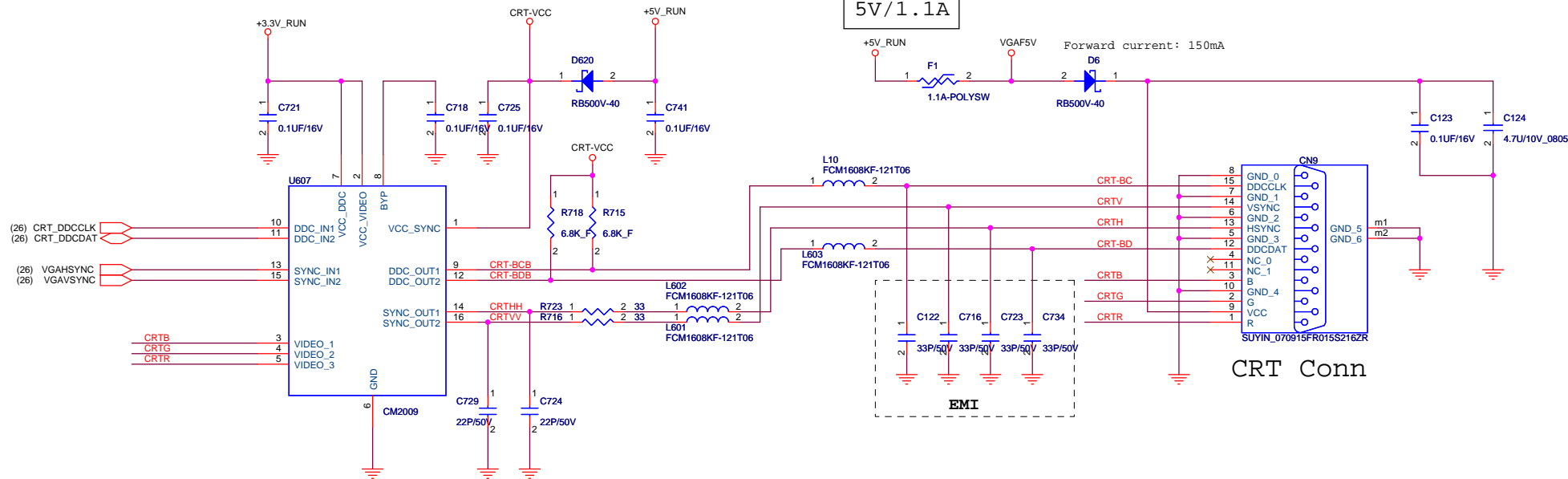
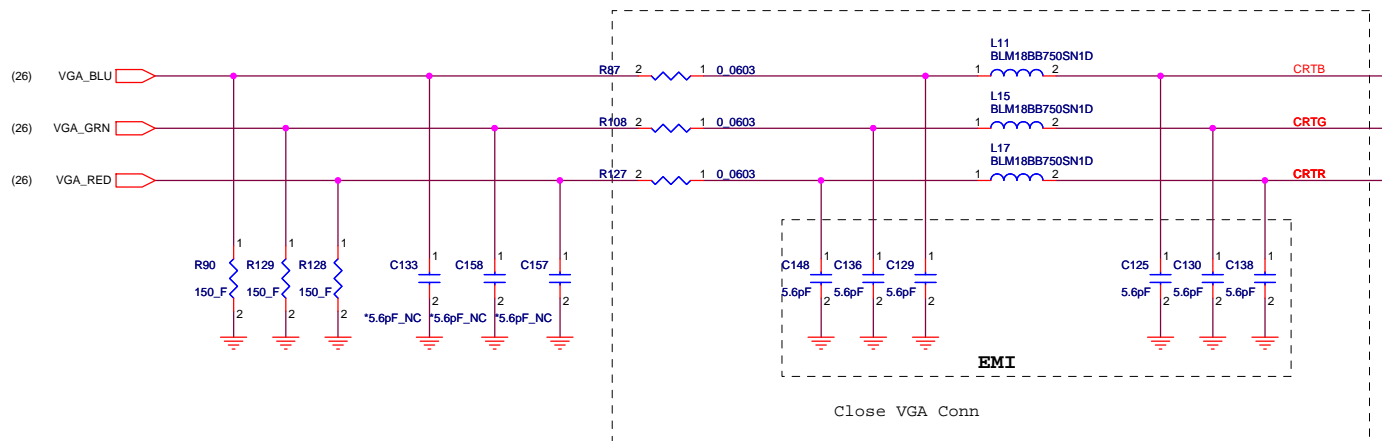
# Embedded DISPLAY PORT CONNECTOR



A	B	C	D	E
4				
3				
2				
1				

Title		
HDMI SELECTION		
Size	Document Number	
	Dell/FLEX Confidential	
Date:	Thursday, October 22, 2009	Sheet 30 of 68
		Rev X02

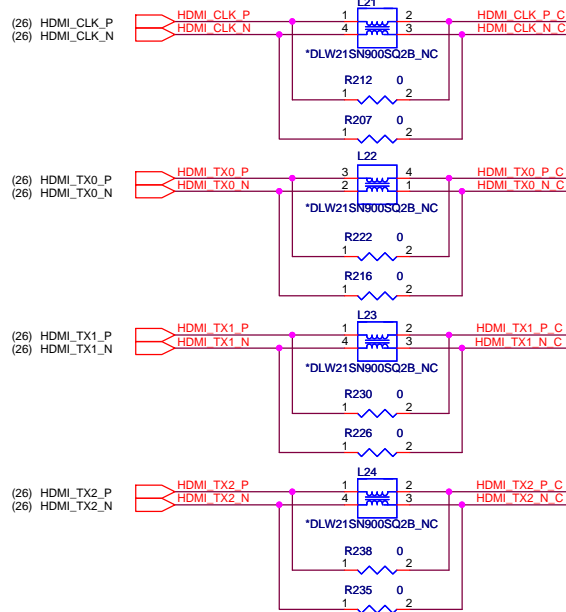




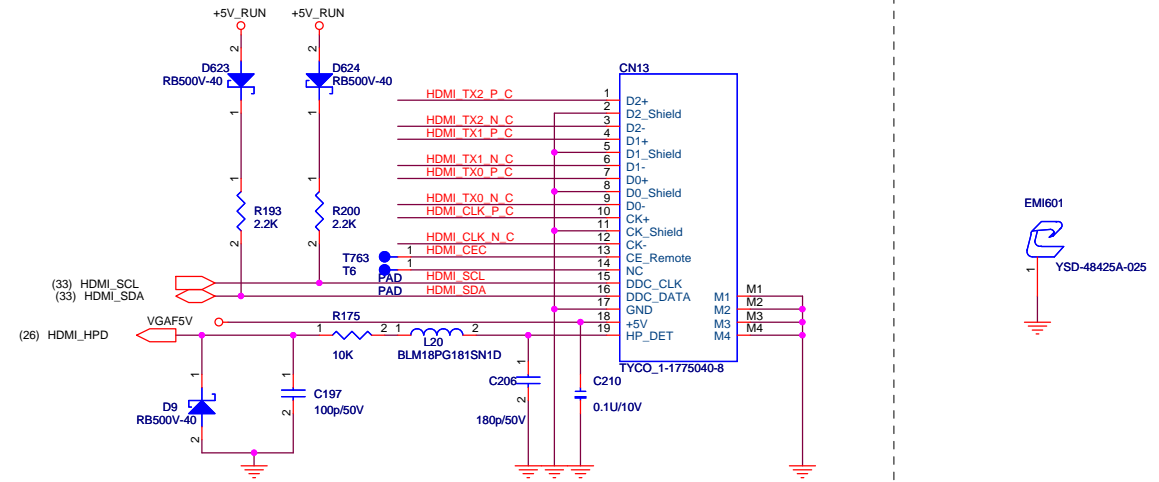




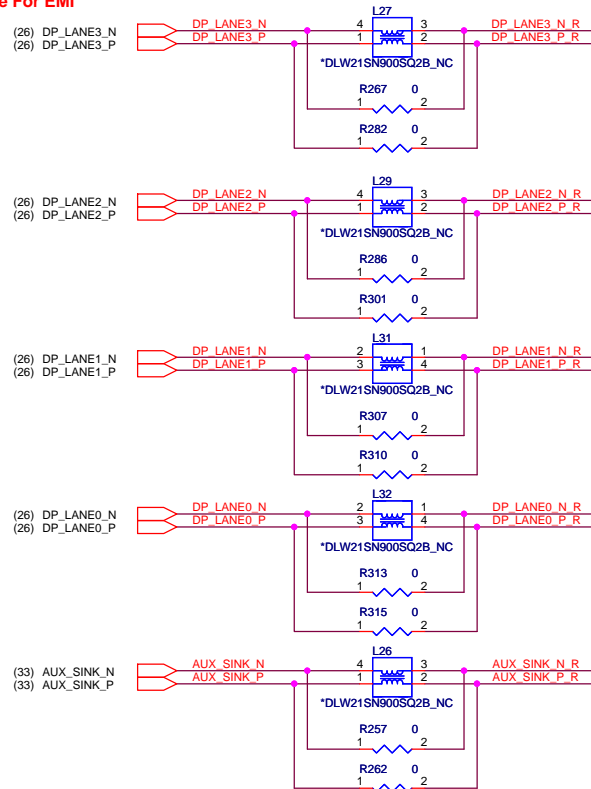
### Reserve For EMI



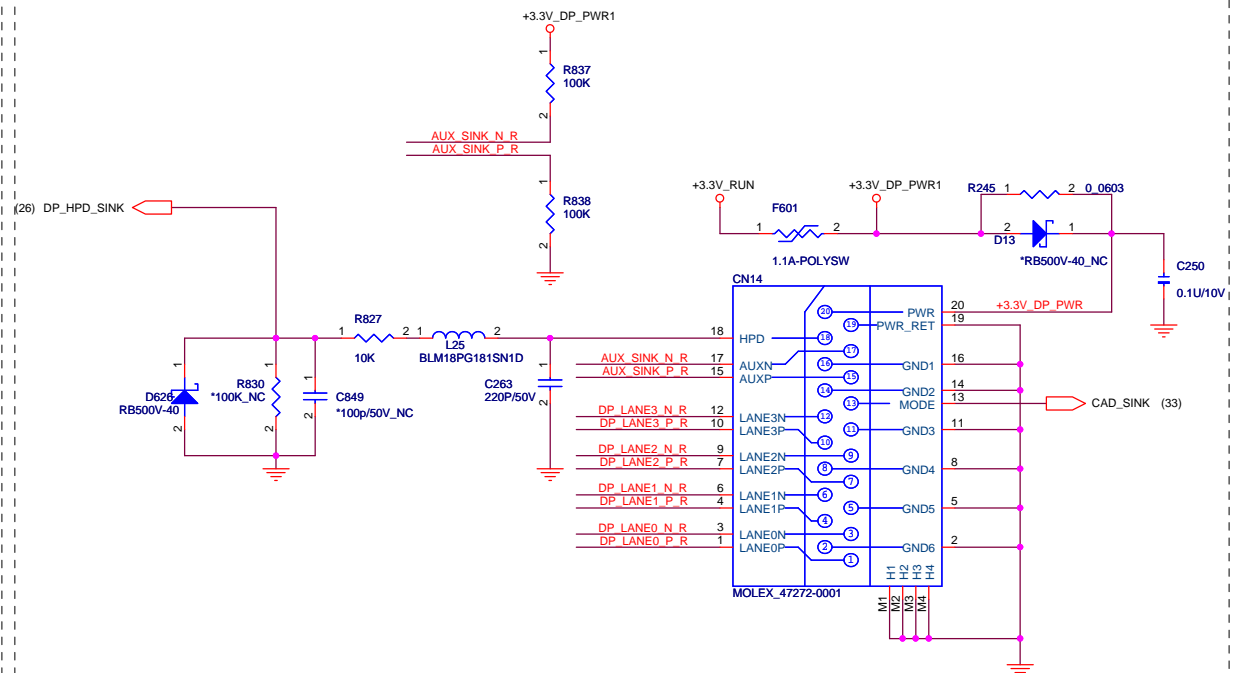
## HDMI CONNECTOR



**Reserve For EMI**



## DISPLAY PORT CONNECTOR



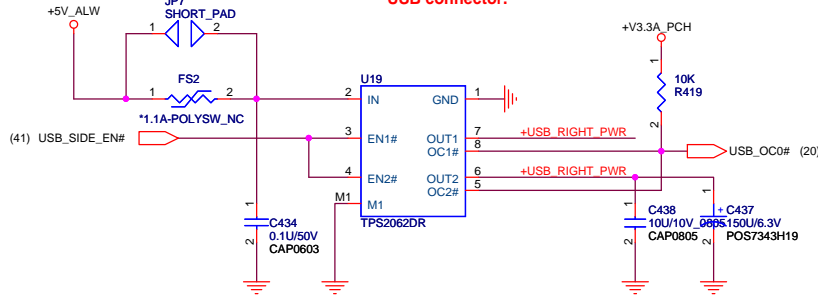
Title			
<b>HDMI &amp; DP CONN</b>			
Size	Document Number	Rev	
<b>Dell/FLEX Confidential</b>		<b>X02</b>	
Date:	Thursday, October 22, 2009	Sheet	34 of 68



## USB POWER SW

Place one 150uF cap by each USB connector.

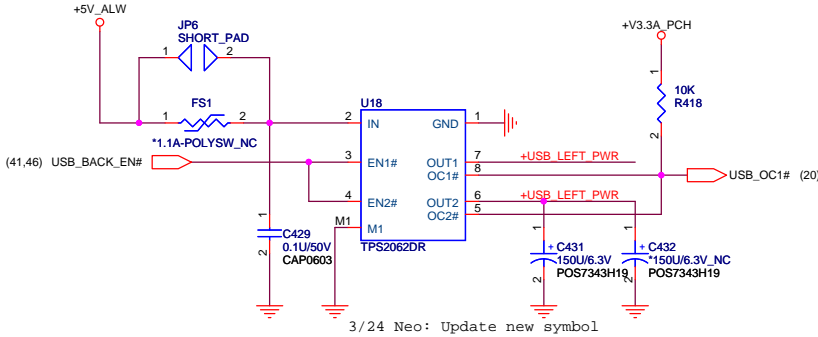
Each channel is 1A



## USB POWER SW

Place one 150uF cap by each USB connector.

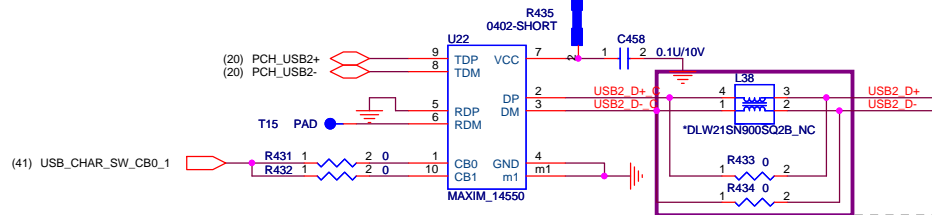
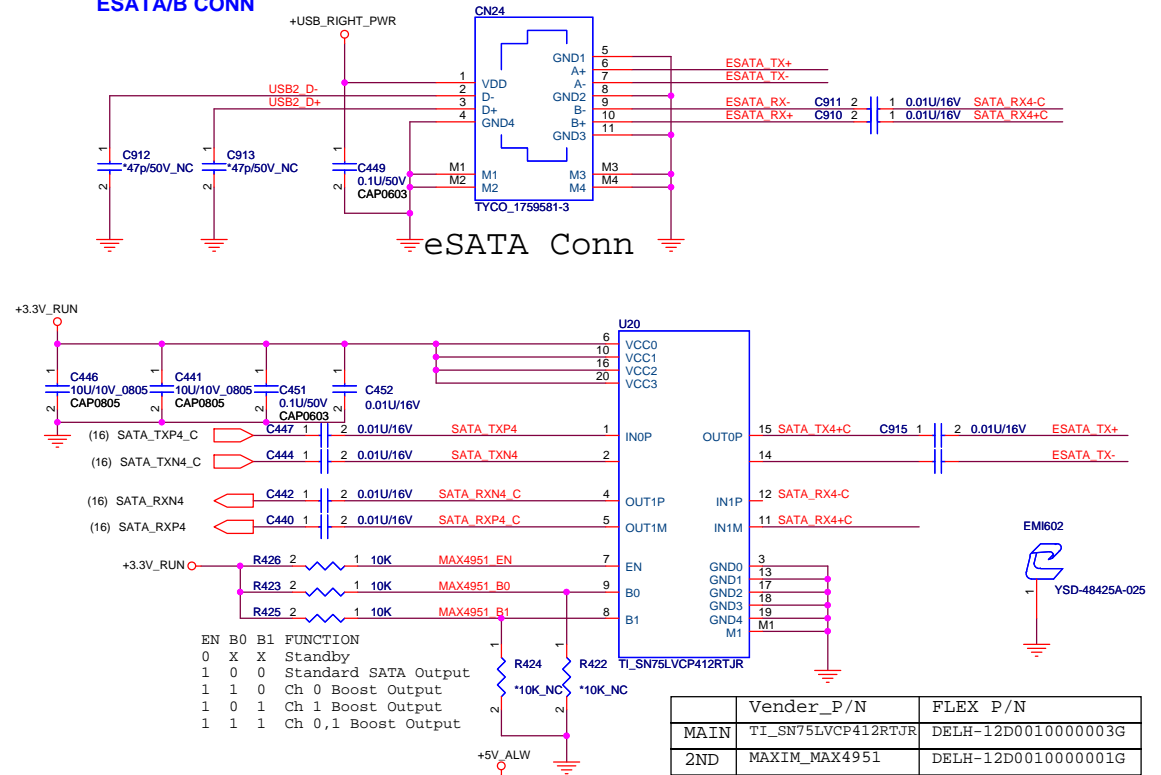
Each channel is 1A



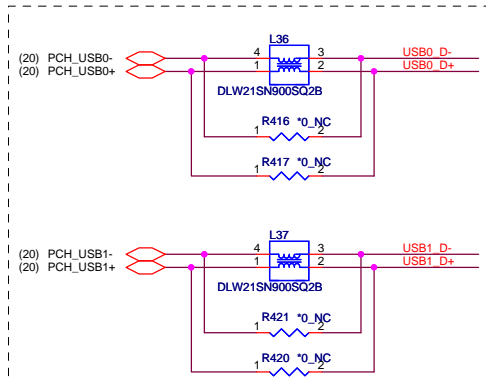
USB\_OC0# C435 1 2 47p/50V

USB\_OC1# C433 1 2 47p/50V

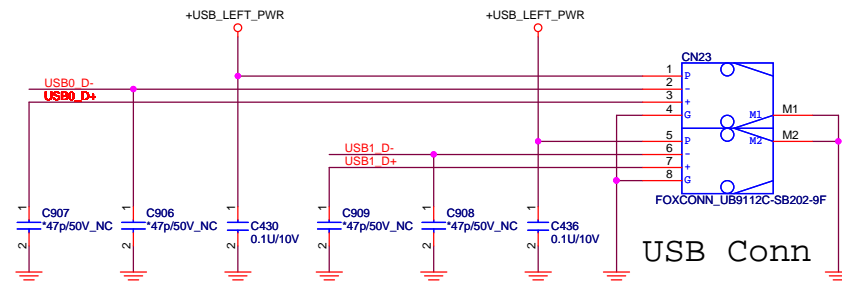
## ESATA/B CONN



## USB CONN

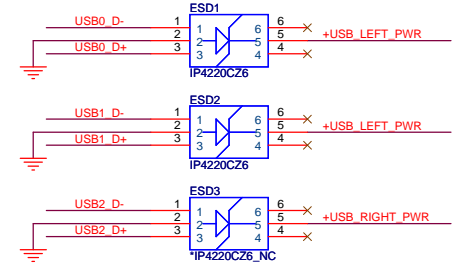


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



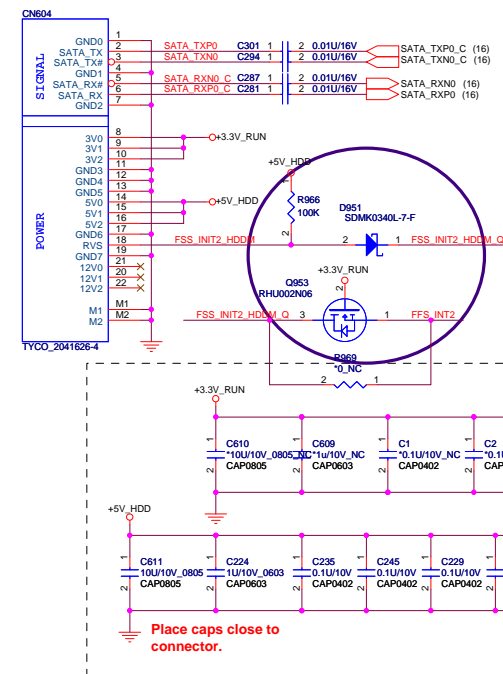
## USB Conn

Place ESD diodes as close as USB connector.

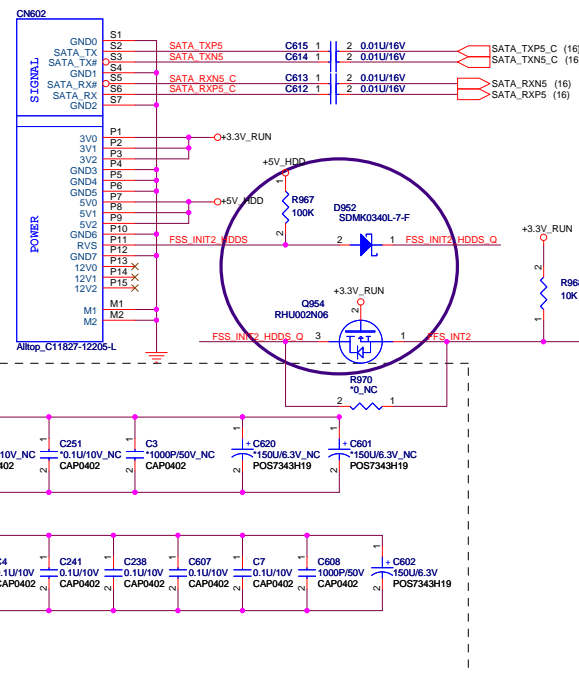


Title		
USBx2 & eSATA		
Size	Document Number	Rev
	Del/FLEX Confidential	X02
Date:	Thursday, October 22, 2009	Sheet 36 of 68

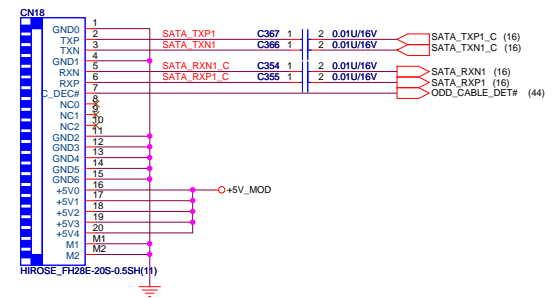
## SATA Connector Master HDD Conn



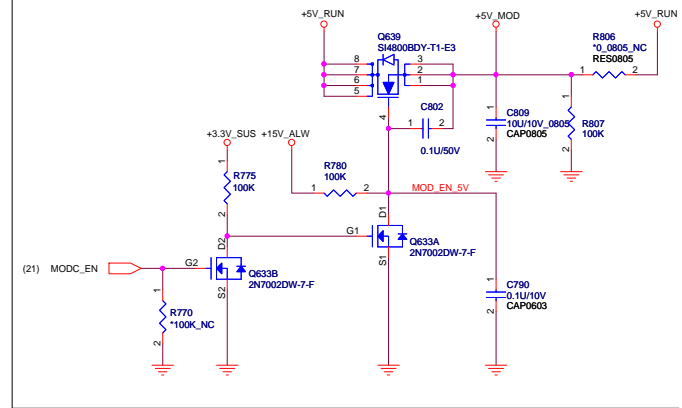
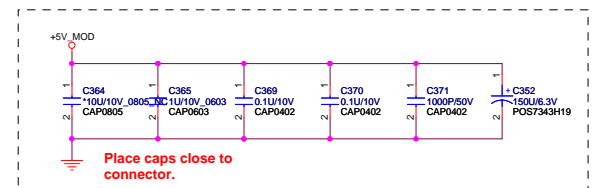
## Slave HDD Conn



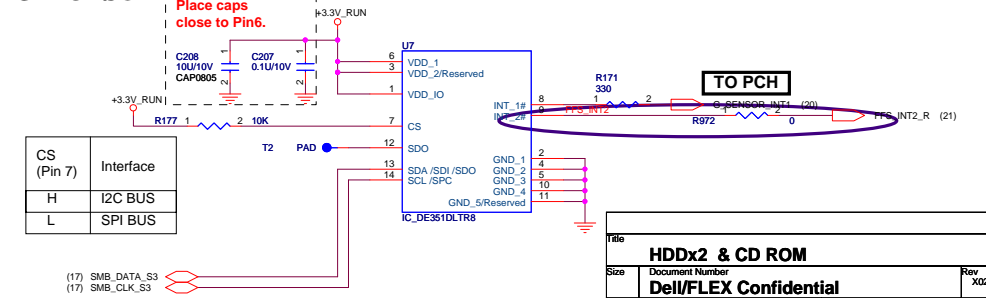
## ODD Connector



## ODD Conn

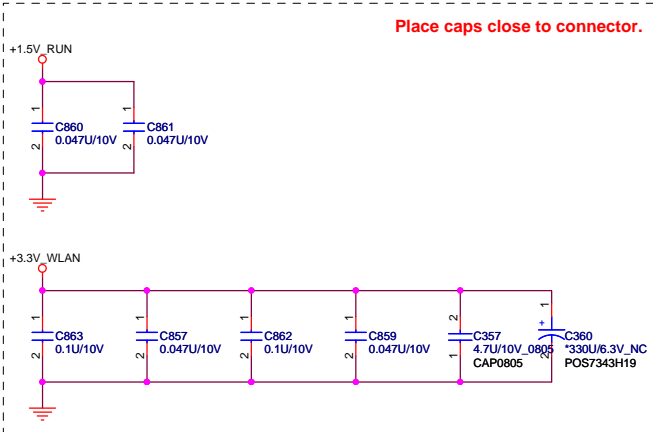
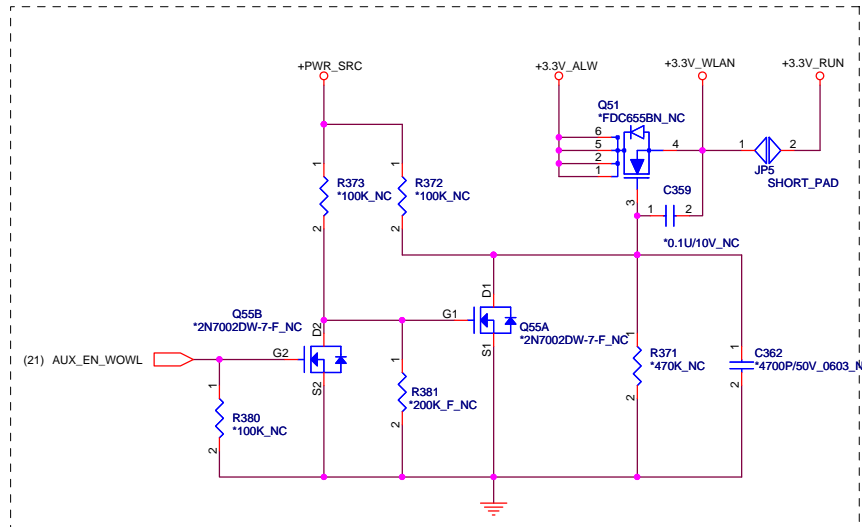
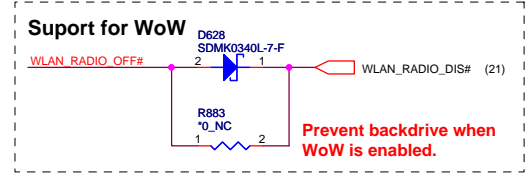
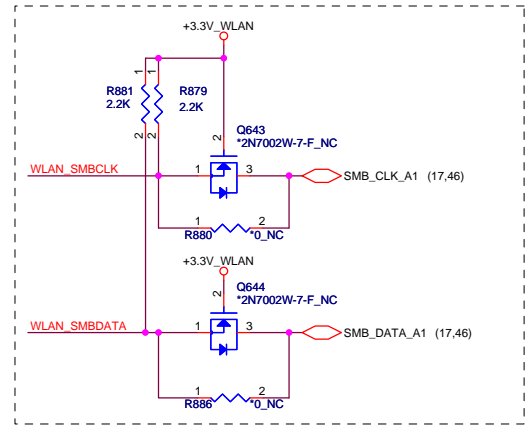
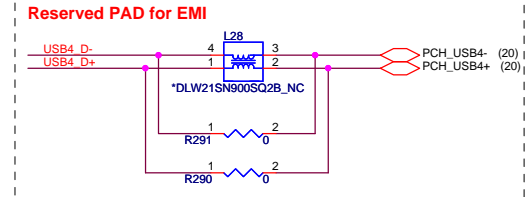
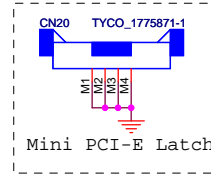
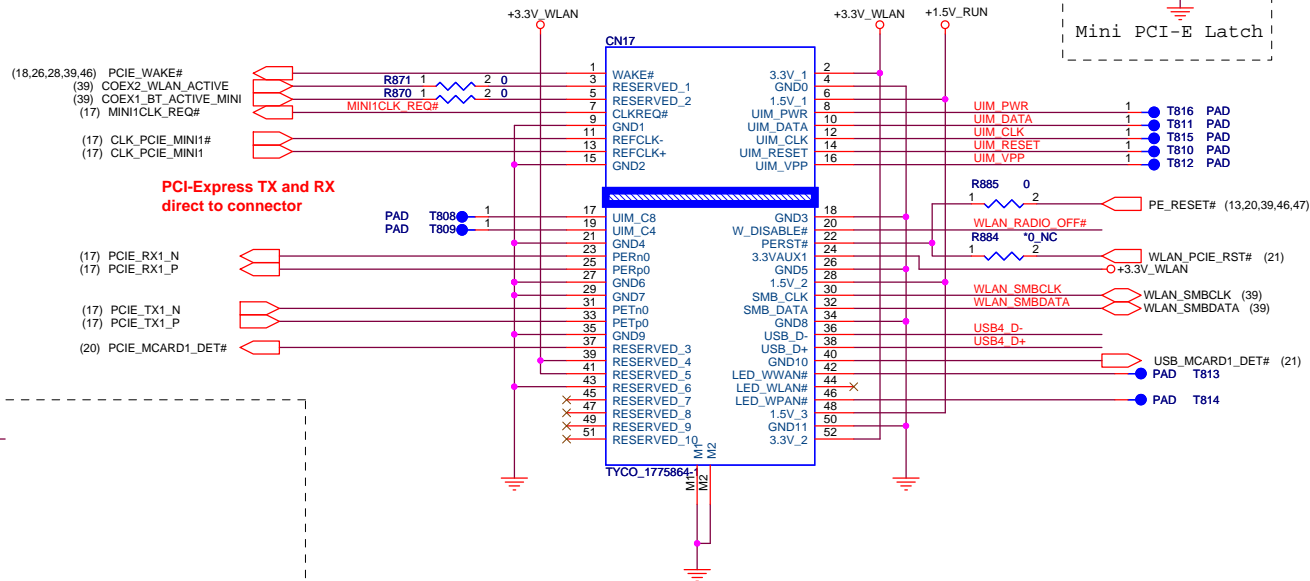


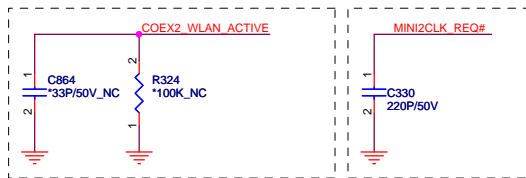
## G-Sensor



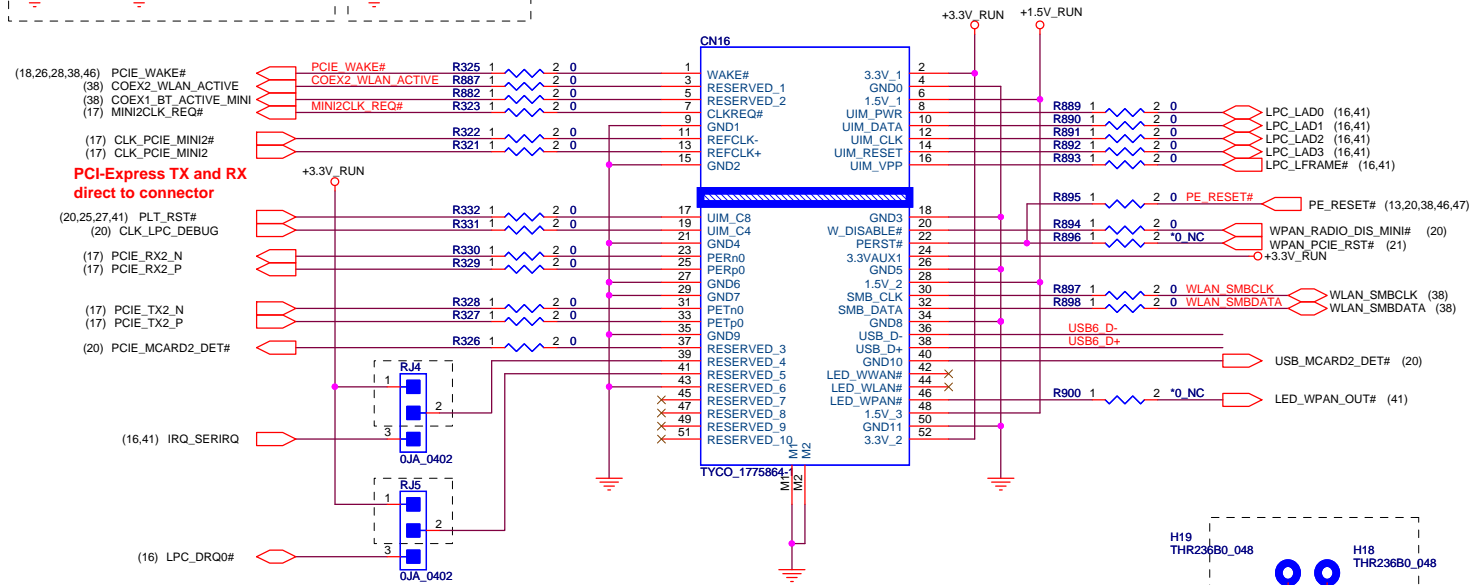
CS (Pin 7)	Interface
H	I2C BUS
L	SPI BUS

## MiniCard WMAX Connector



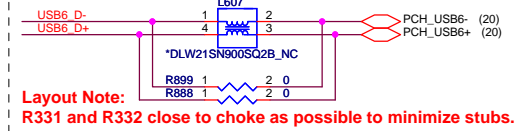


## Flash Cache Module, BT, UWB Connector



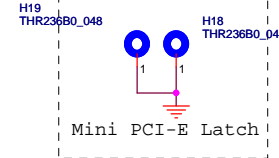
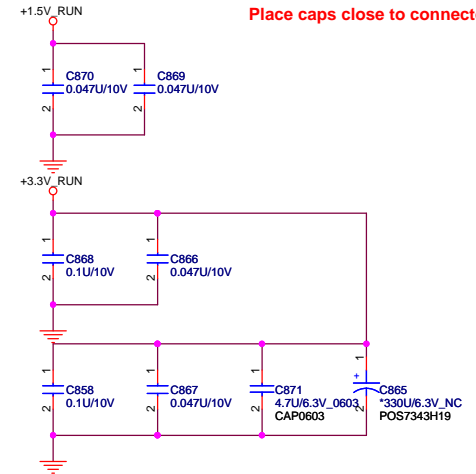
## MiniCard WWAN Connector

### Reserve For EMI



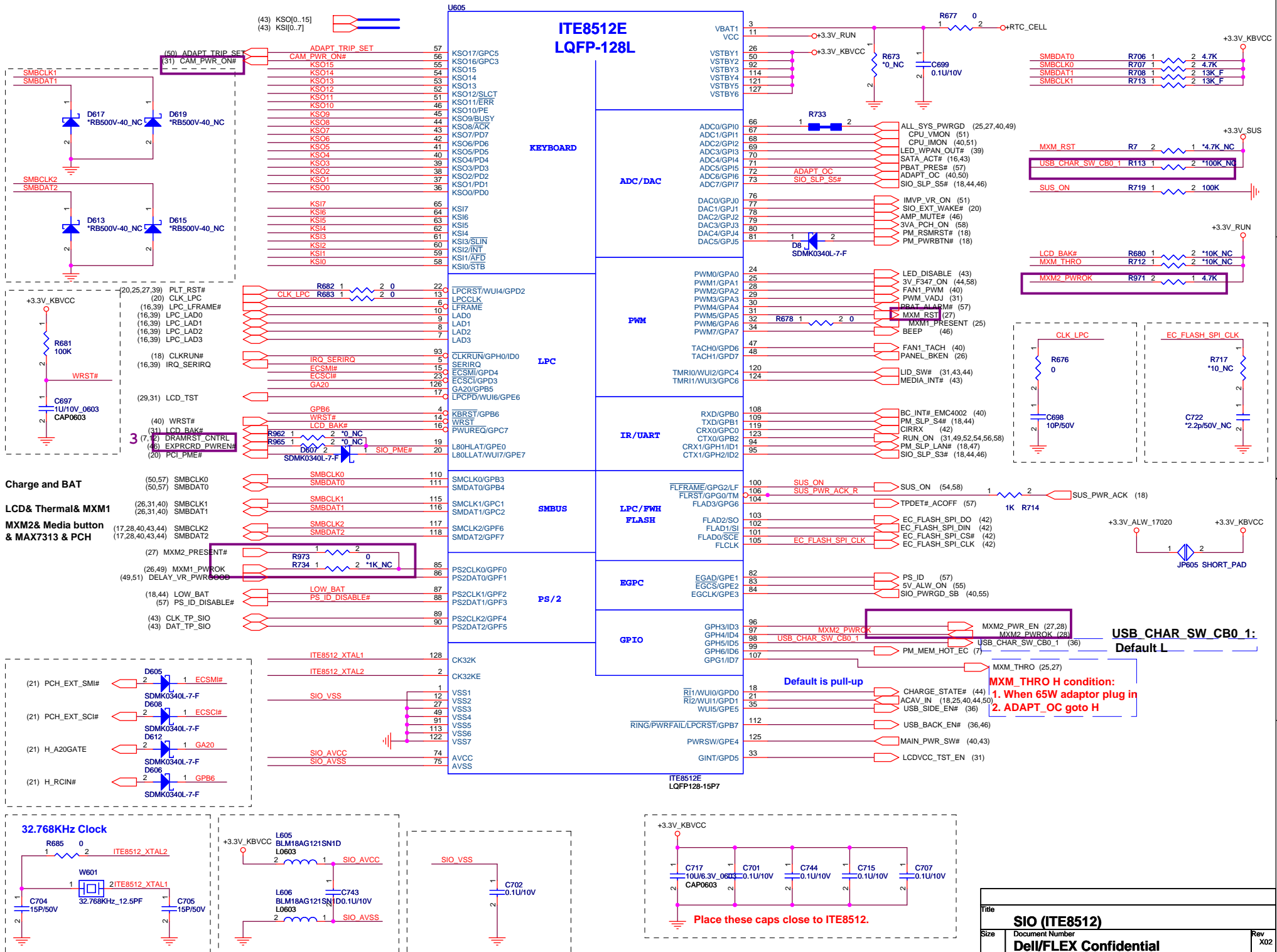
**Layout Note:**  
R331 and R332 close to choke as possible to minimize stubs.

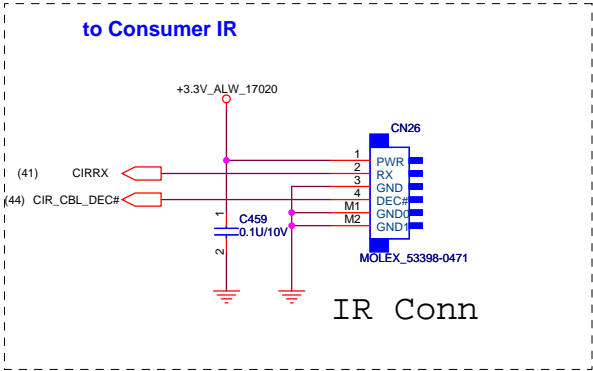
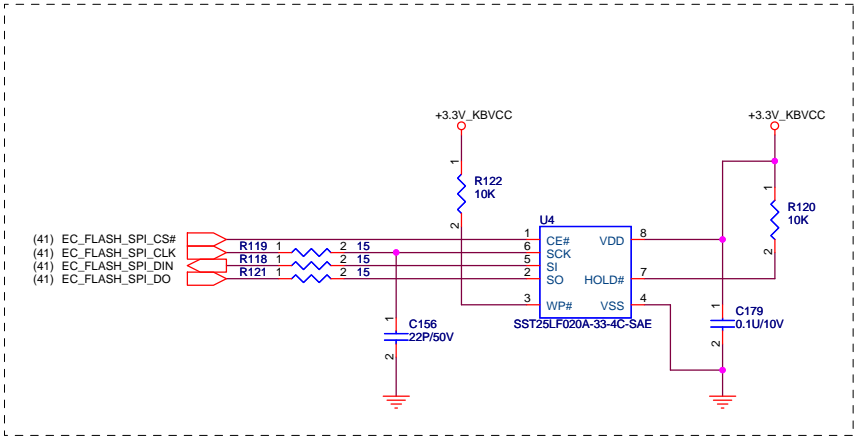
**Place caps close to connector.**



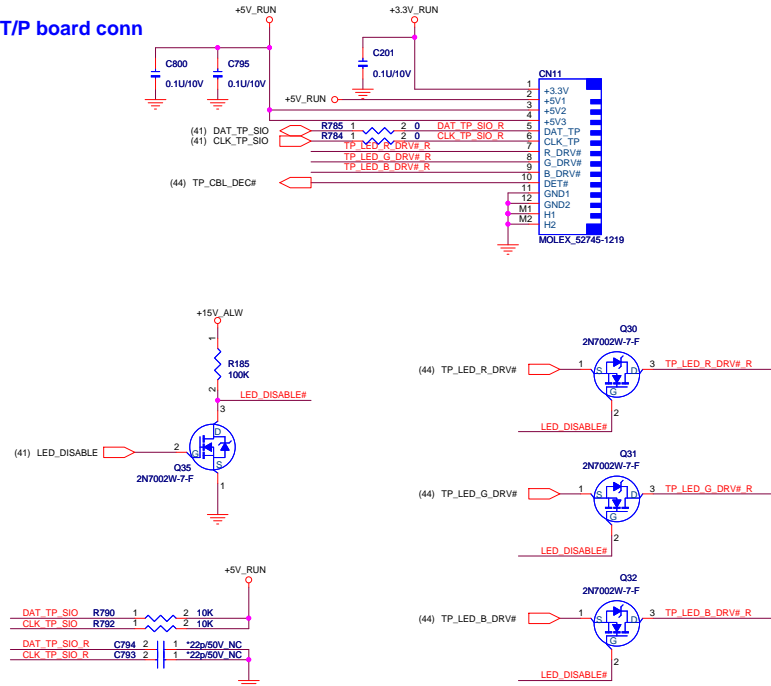




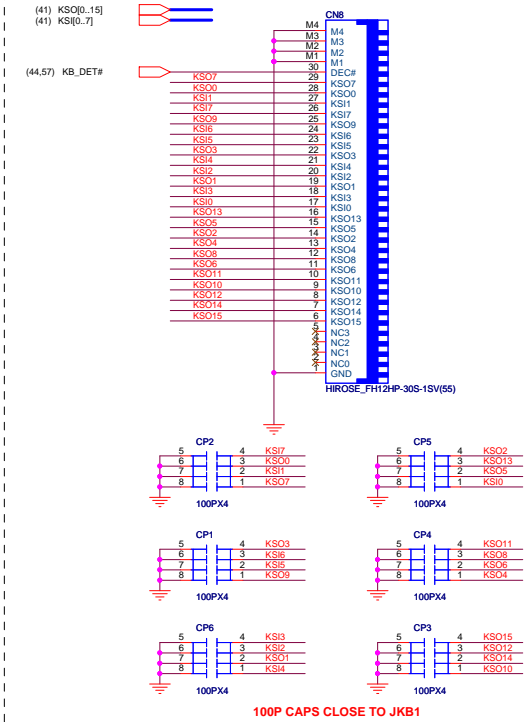




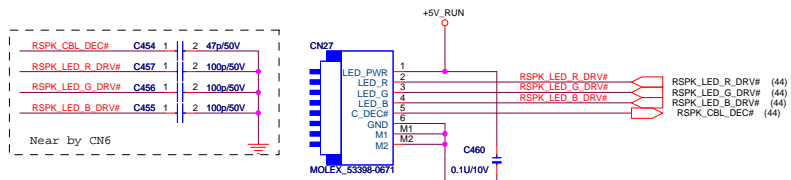
## T/P board conn



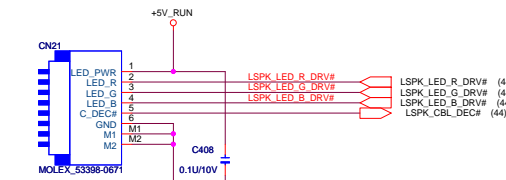
## KEYBOARD CONNECTOR



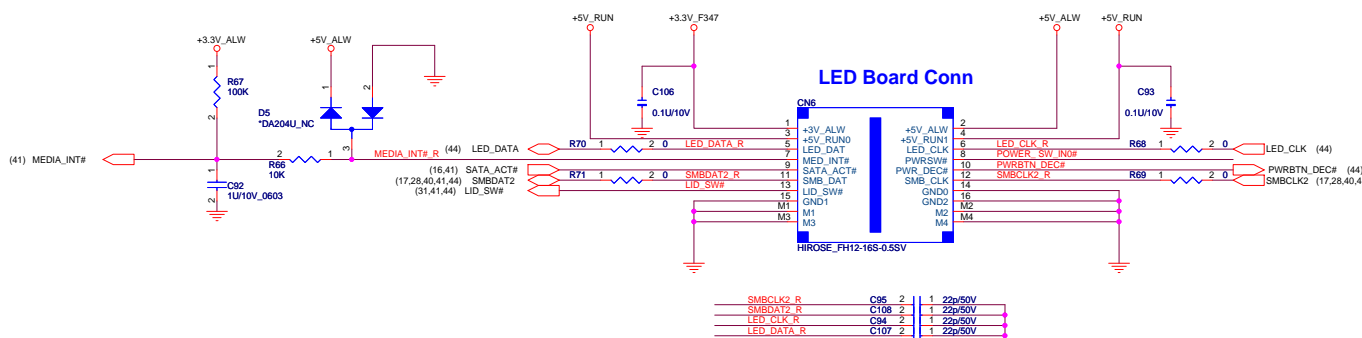
## Right SPK LED Conn



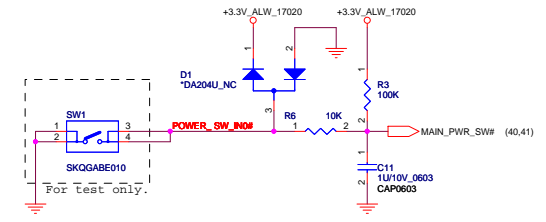
## Left SPK LED Conn

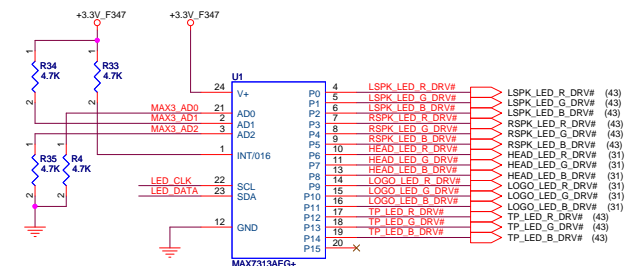
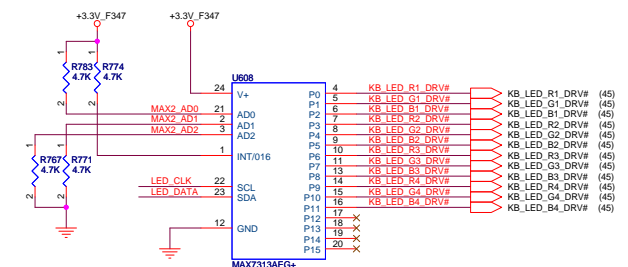
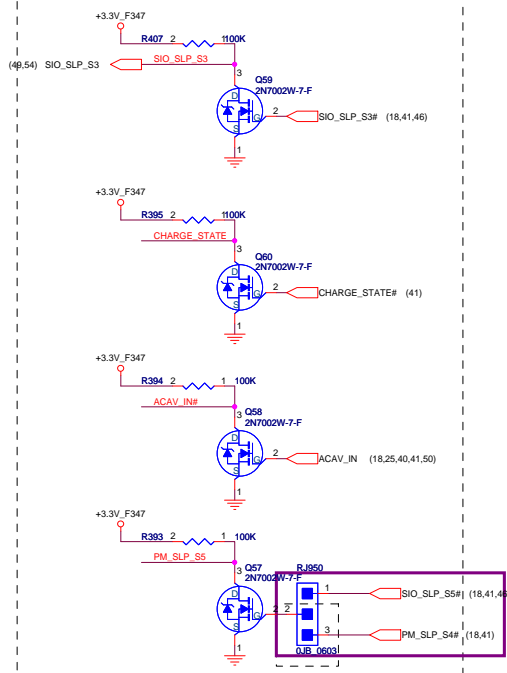
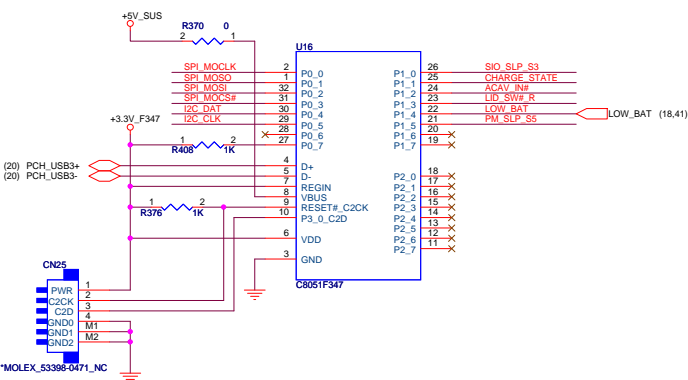
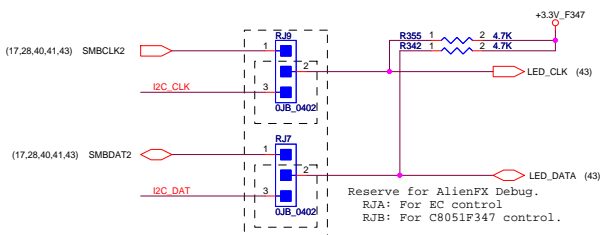
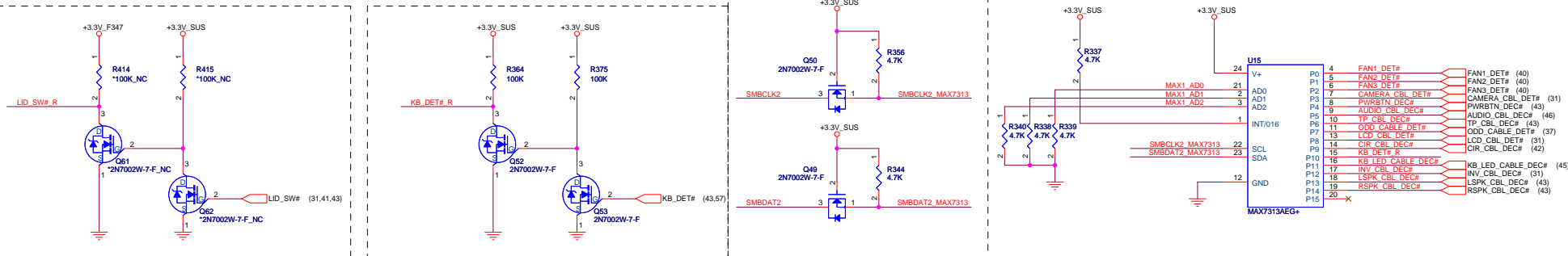


## LED Board Conn



## Power Button

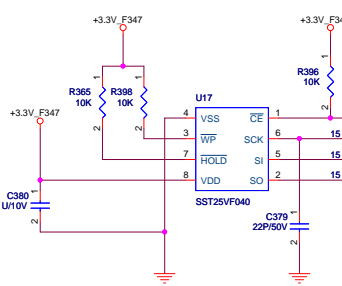




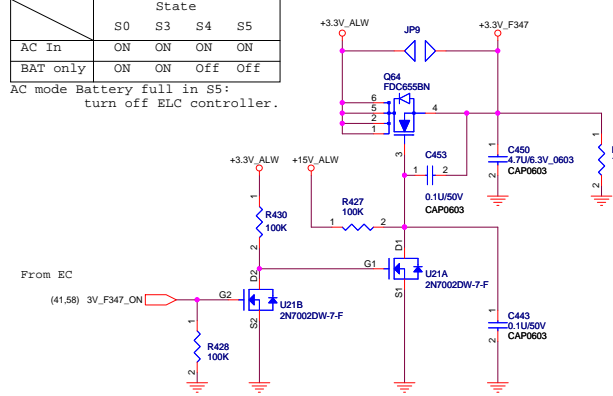
+3.3V\_F347 behavior

	State			
	S0	S3	S4	S5
AC In	ON	ON	ON	ON
BAT only	ON	ON	Off	Off

AC mode Battery full in S5:  
turn off ELC controller.

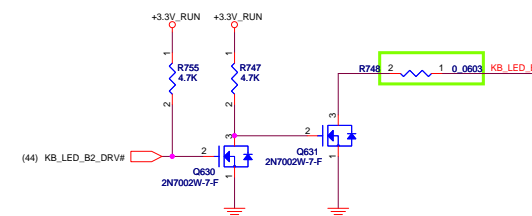
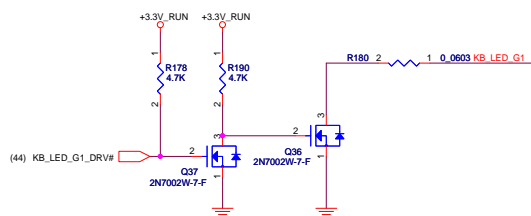
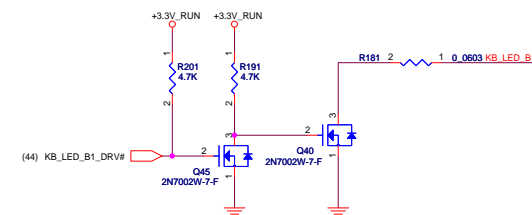
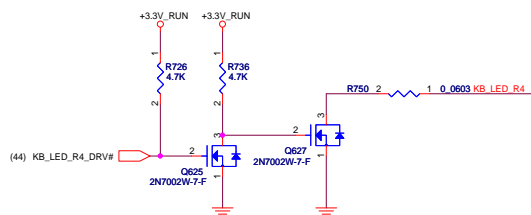
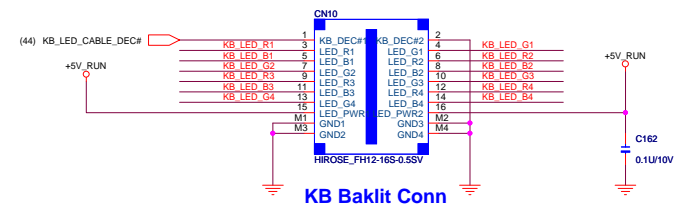
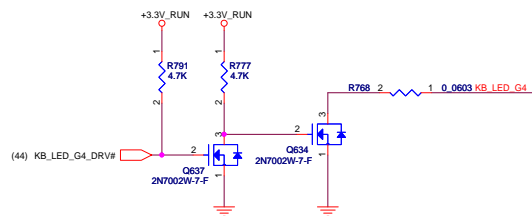
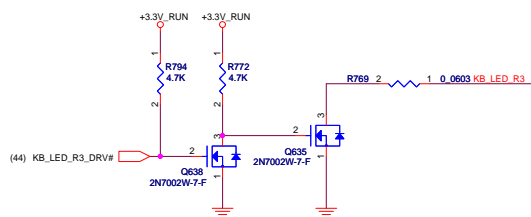
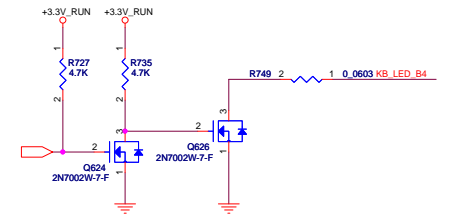
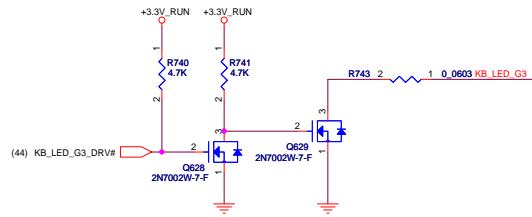
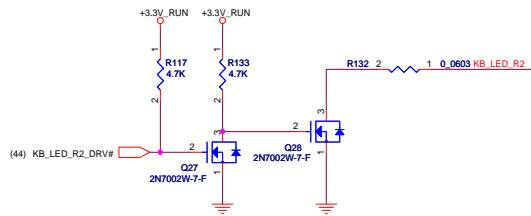
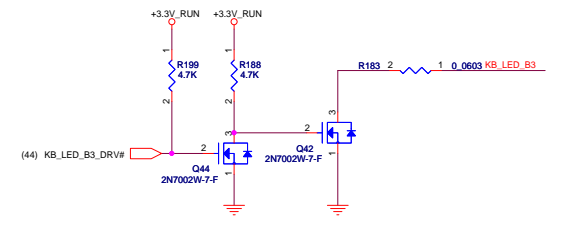
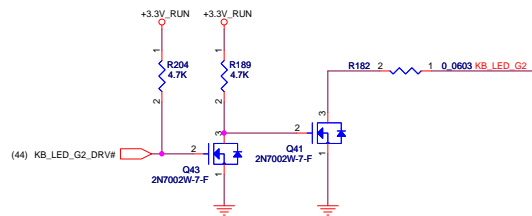
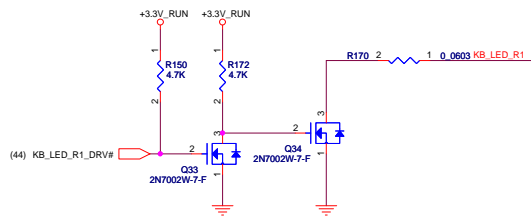


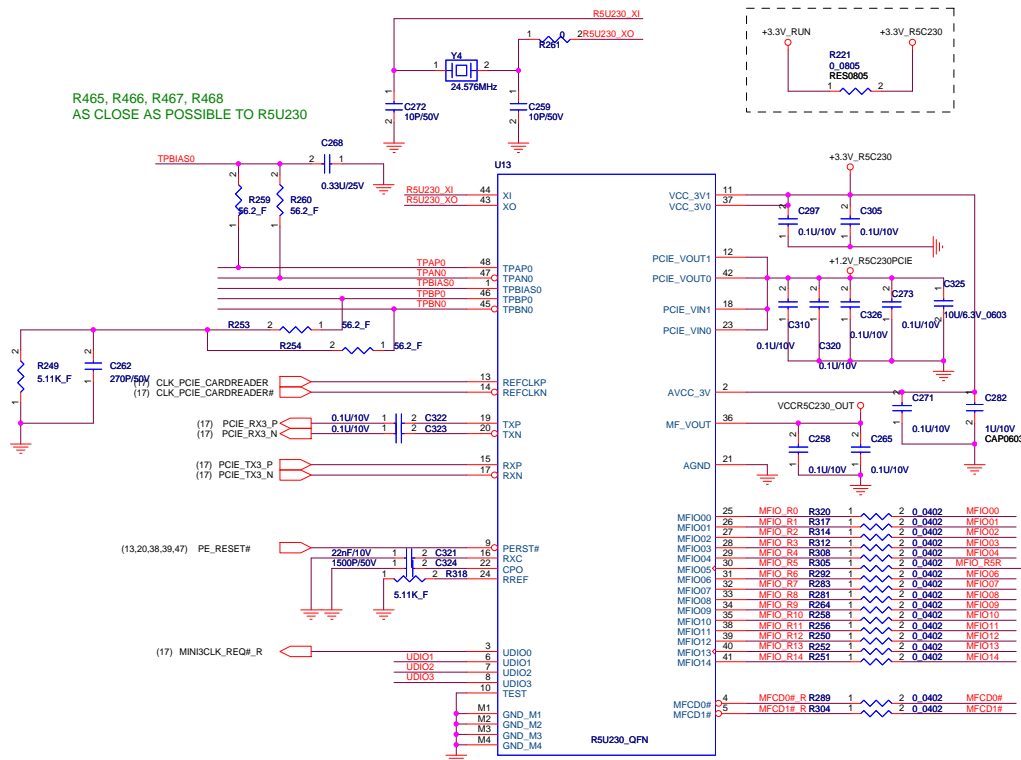
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM (U40)	1010 000b



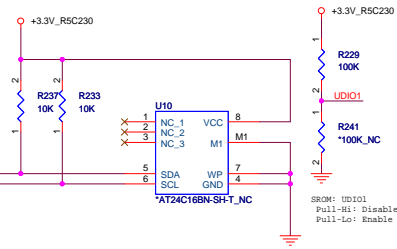
Reference	AD2	AD1	AD0	MAX7313 #
U41	0	0	0	Cable Detect#
U43	0	0	1	KB LED
U45	0	1	0	SPK& Head& Logo& T/P LED
---	0	1	1	LED Board
---	1	0	0	Media Board
---	1	0	1	Media Board

CAMERA_CBL_DET#	R354	1	2	100K
AUDIO_CBL_DEC#	R362	1	2	100K
TP_CBL_DEC#	R368	1	2	100K
ODD_CBL_DET#	R374	1	2	100K
LCD_CBL_DET#	R383	1	2	100K
CIR_CBL_DEC#	R361	1	2	100K
KB_LED_CBL_DEC#	R357	1	2	100K
FAN1_DET#	R443	1	2	100K
FAN2_DET#	R347	1	2	100K
FAN3_DET#	R352	1	2	100K
INV_CBL_DEC#	R353	1	2	100K
LSPK_CBL_DEC#	R348	1	2	100K
RSPK_CBL_DEC#	R346	1	2	100K
PWRBTN_DEC#	R358	1	2	100K

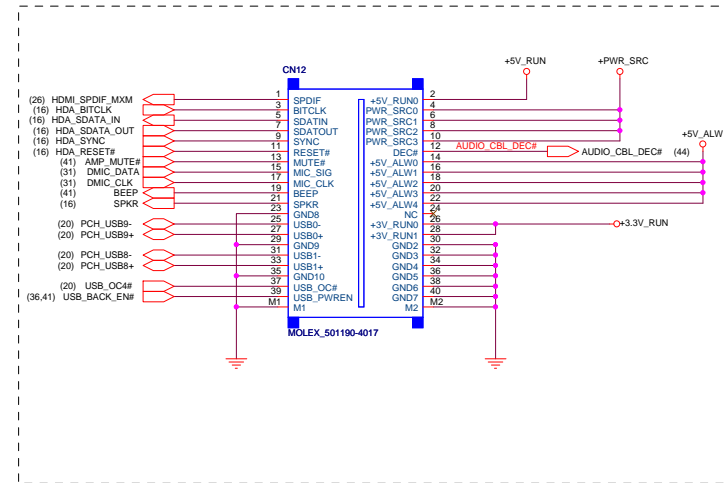
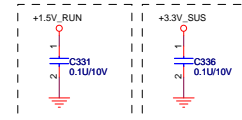
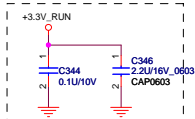
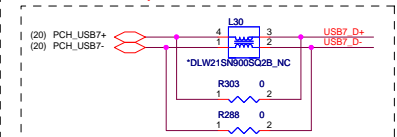


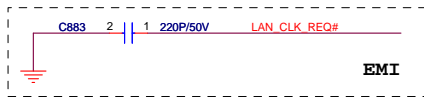


- Reserved EMI Solution**
- TPBNO 1 L39 2 QLTBP- CN28 M1  
TPBP0 1 QLTBP- 2 QLTBP+ M1
- DLW21SN181SQ2
- TPANO 1 L40 2 QLTAP- M2  
TPAPO 1 QLTAP- 2 QLTAP+ M2
- DLW21SN181SQ2
- MOLEX\_54030-0471

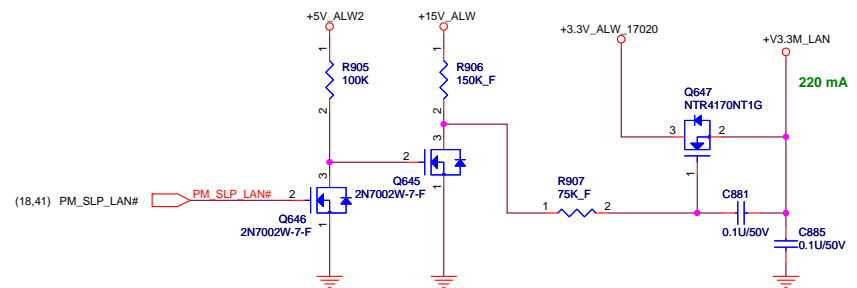
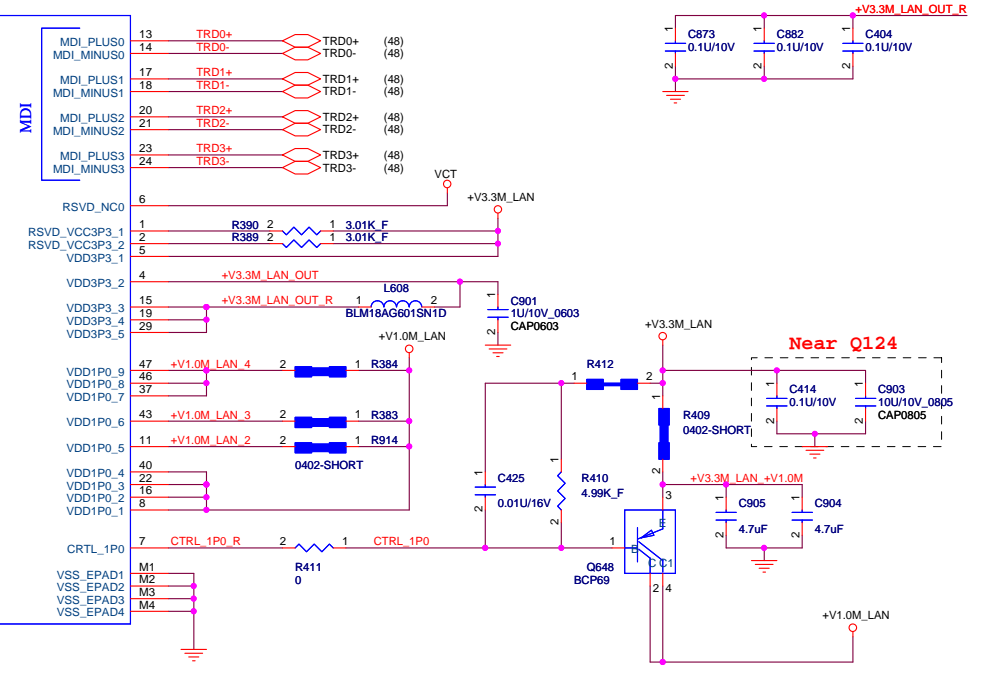
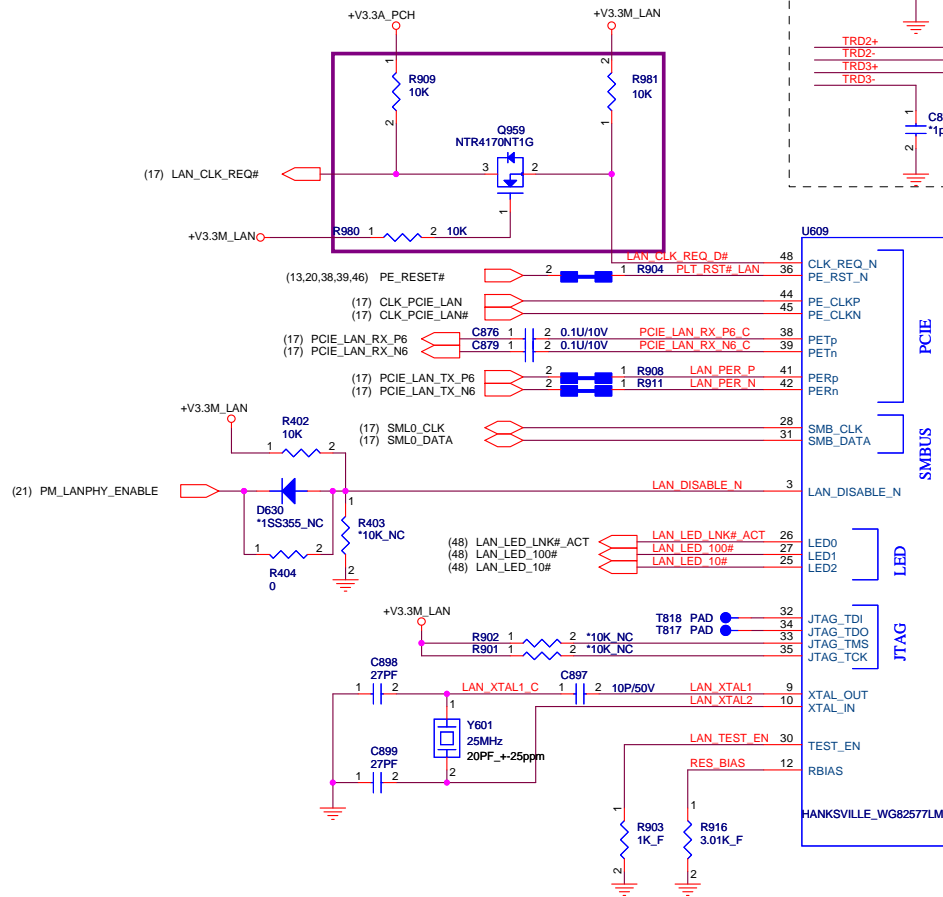
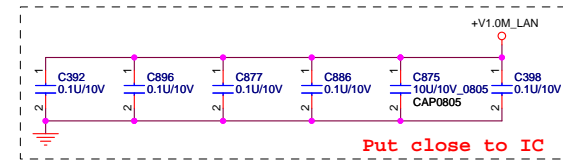
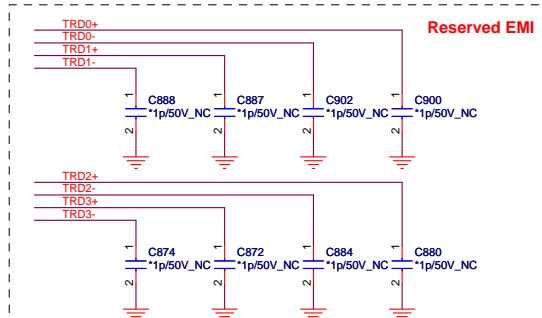


MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	-
02	D0	D5	D1
03	D7	D4	-
04	D6	D3	D5
05	CLK	D2	D0
06	-	D1	-
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	-
12	-	CE#	-
13	-	RE#	D7
14	-	R/B#	CLK
MFCD0#	CD8	CD0#	-
WFCd1#	-	CD1#	IN0#

[illegible]



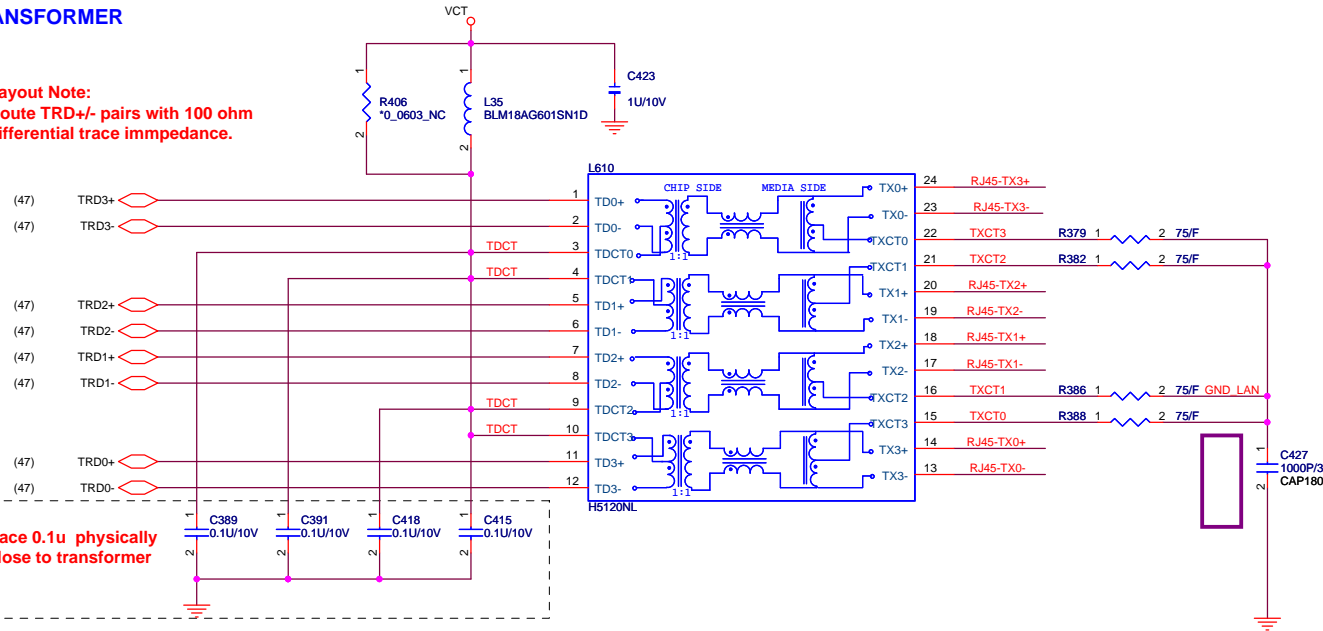
Hanksville PHY	FLEX P/N
WG82577LC QKPN	DELH-10D0040000005G



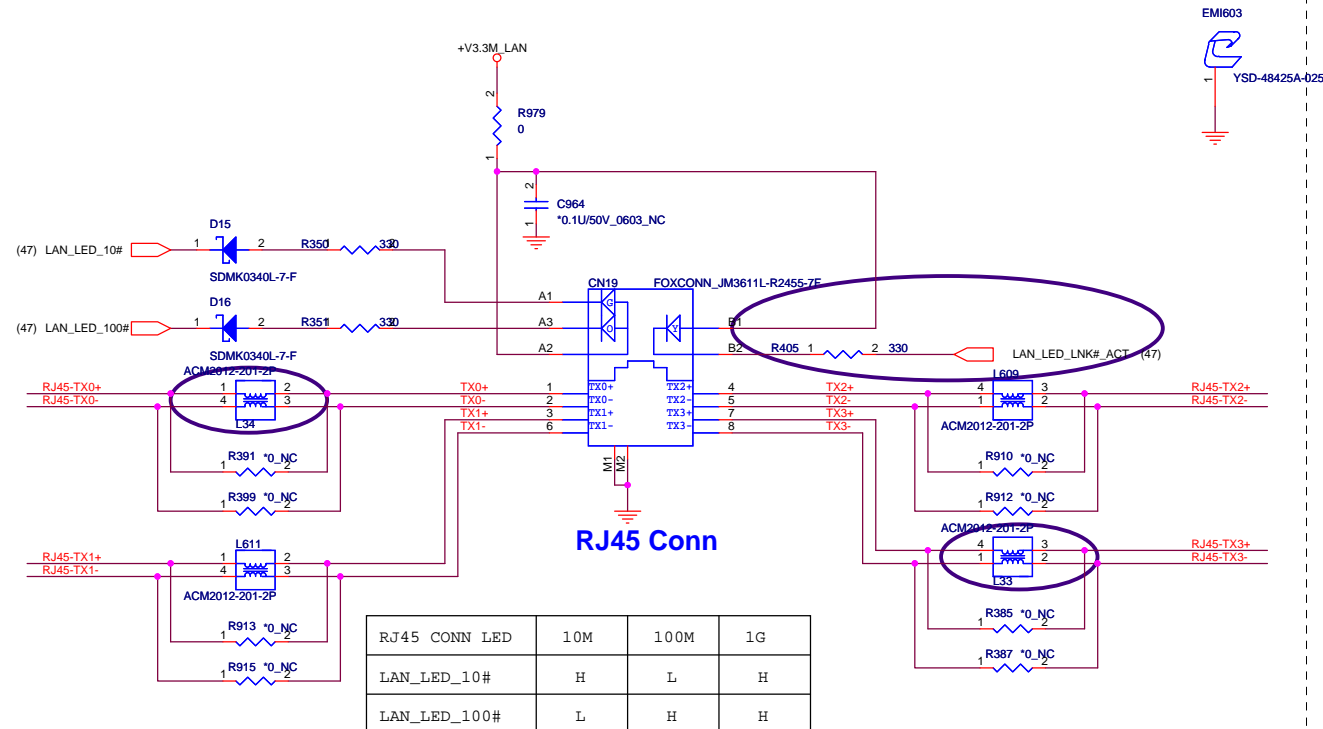


## TRANSFORMER

**Layout Note:**  
Route TRD+/- pairs with 100 ohm differential trace impedance.



## RJ-45 Connector



RJ45 CONN LED	10M	100M	1G
LAN_LED_10#	H	L	H
LAN_LED_100#	L	H	H



Note:  
Component Values on Schematic are for MAX8731 only,  
Please see table 1-3 for BQ24745 or ISL88731  
component Values.

TABLE 3 . PIN NAME DIFFERENCES

PIN	MAX8731A	ISL88731	bq24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	INP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBISA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSIN	CSIN
18	CSIP	CSOP	CSOP
20	DLO	LAOTE	LAOTE
21	LDO	VDOP	VDOP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGATE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

"NC" means no-connect

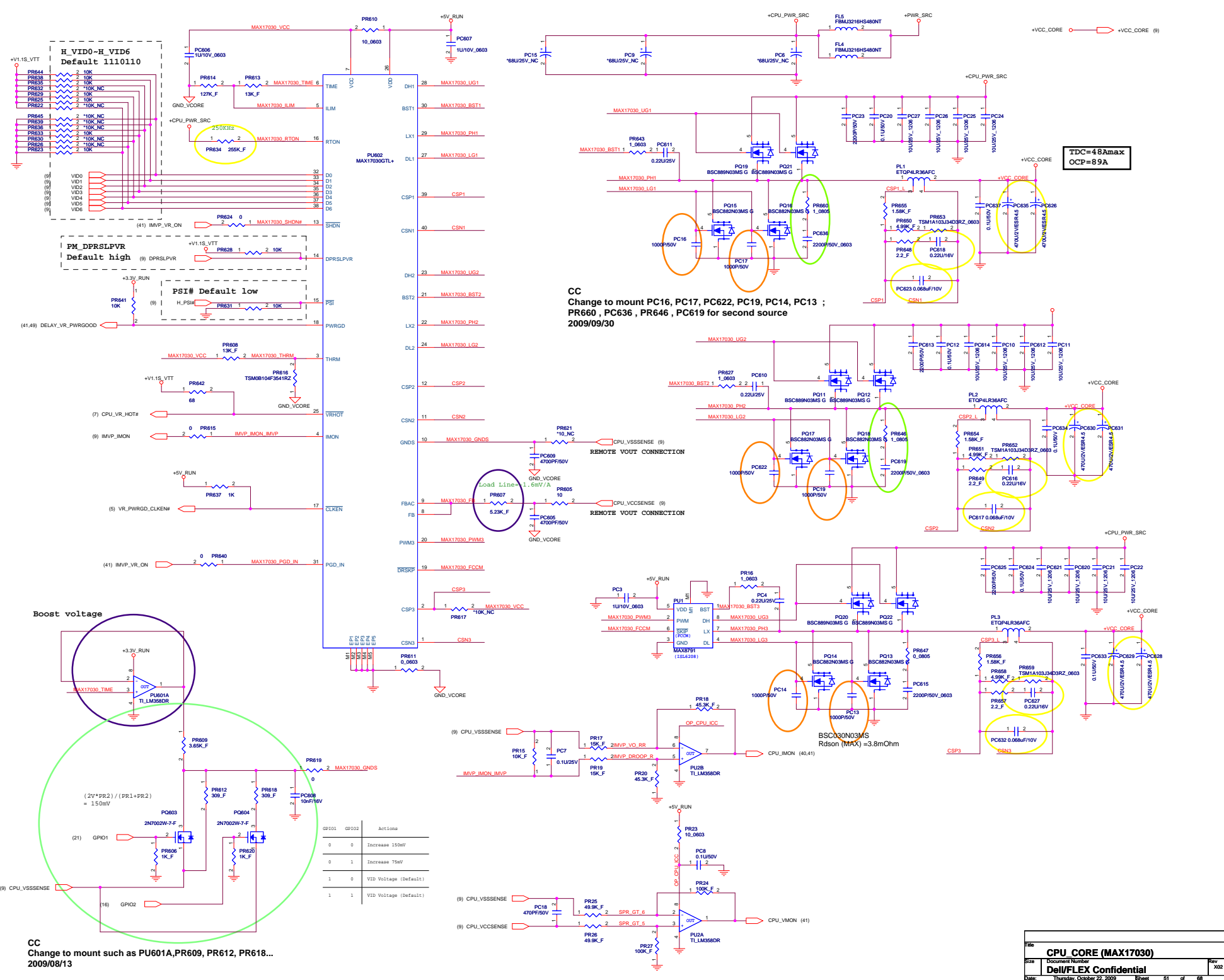
TABLE 2

REF DES	MAXIM	INTERSIL	TI
PR245	NO STUFF	10K, 0402, 5%	NO STUFF
PR227	0, 0402, 5%	10, 0402, 5%	0, 0402, 5%
PR228	0, 0402, 5%	10, 0402, 5%	0, 0402, 5%
PC157	NO STUFF	0.1uF	0.1uF
PC202	NO STUFF	NO STUFF	0.1uF
PC203	NO STUFF	NO STUFF	NO STUFF
PR230	0, 0402, 5%	10, 0402, 5%	0, 0402, 5%
PR231	0, 0402, 5%	10, 0402, 5%	0, 0402, 5%
PC207	NO STUFF	NO STUFF	0.1uF
PC208	NO STUFF	0.1uF	0.1uF
PC209	NO STUFF	NO STUFF	NO STUFF
PR17	8.2K, 0402, 5%	2.2K, 0402, 5%	4.7K, 0402, 5%
PR18	8.45K, 0402, 1%	NO STUFF	NO STUFF
PR232	NO STUFF	NO STUFF	200K, 0402, 5%
PR233	NO STUFF	NO STUFF	7.5K, 0402, 5%
PR234	NO STUFF	0, 0402, 5%	NO STUFF
PC23	0.1uF, 0402, 10V	NO STUFF	200uF, 0402, 10V
PC24	0.01uF	0.01uF	NO STUFF
PC210	NO STUFF	NO STUFF	130uF, 0402, 10V
PC211	0.01uF	NO STUFF	NO STUFF
PC153	0.01uF	0.01uF	NO STUFF
PC204	NO STUFF	NO STUFF	51uF, 0402, 10V
PC206	NO STUFF	NO STUFF	2000uF, 0402, 10V
PC27	1.0uF, 0603, 10V	NO STUFF	1.0uF, 0603, 10V
PC28	0.1uF, 0402, 10V	NO STUFF	NO STUFF
PR10	10K, 0402, 1%	10K, 0402, 1%	NO STUFF
PR7	15.8K, 0402, 1%	15.8K, 0402, 1%	NO STUFF
PR229	NO STUFF	NO STUFF	10K, 0402, 5%
PR5	365K, 0402, 1%	215K, 0402, 1%	309K, 0402, 1%
PR1	CH501H-40P1	CH501H-40P1	CH501H-40P1
PR6	33, 0603, 1%	33, 0603, 1%	NO STUFF
PC11	1.0uF, 0603, 10V	1.0uF, 0603, 10V	NO STUFF
PR12	1, 0603, 1%	0, 0603, 5%	0, 0603, 5%
PR16	100, 0402, 5%	100, 0402, 5%	0, 0402, 5%
PC22	220uF, 0402, 50V	NO STUFF	NO STUFF
PR239	0, 0402, 5%	8.45K, 0402, 1%	8.45K, 0402, 1%
PC214	0.01uF	0.1uF	0.1uF
PC12	3.3uF	NO STUFF	NO STUFF

TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	MAX8731A/ISL88731				bq24745		
		R237	R241	R243	R242 (see Note 1)	R241	R243	R242 (see Note 1)
65	3.17	57.6K	13K	105	24.9K	12.4K	205	24.3K
150	7.43	30.9K	24.9K	499	10.7K	23.7K	499	10.5K
240	11.69 (see Note 2)	17.8K	6.49K	3.48K	2.37K	8.45K	1.18K	23.2K

Note 1 : R242 is populated if ADAPT\_TRIP\_SET is used to program for the next lower adapter  
ADAPT\_TRIP\_SET is floating for the higher adapter, grounded for the lower adapter  
Note 2 : RR1 must be 5mOhms instead of 10mOhms for the 240W adapter



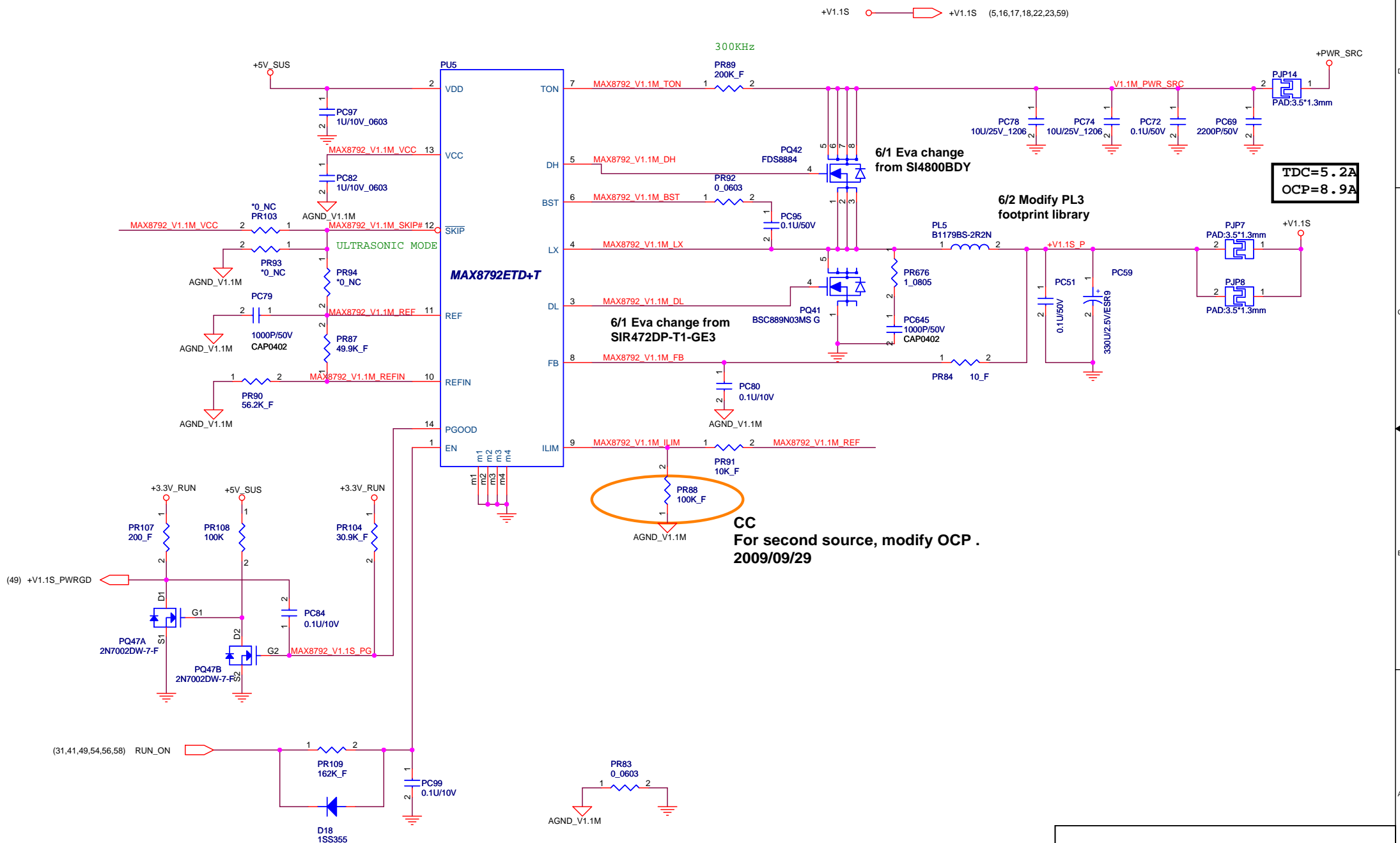
CC  
Change to mount PC16, PC17, PC622, PC19, PC14, PC13 ;  
PR660 , PC636 , PR646 , PC619 for second source  
2009/09/30

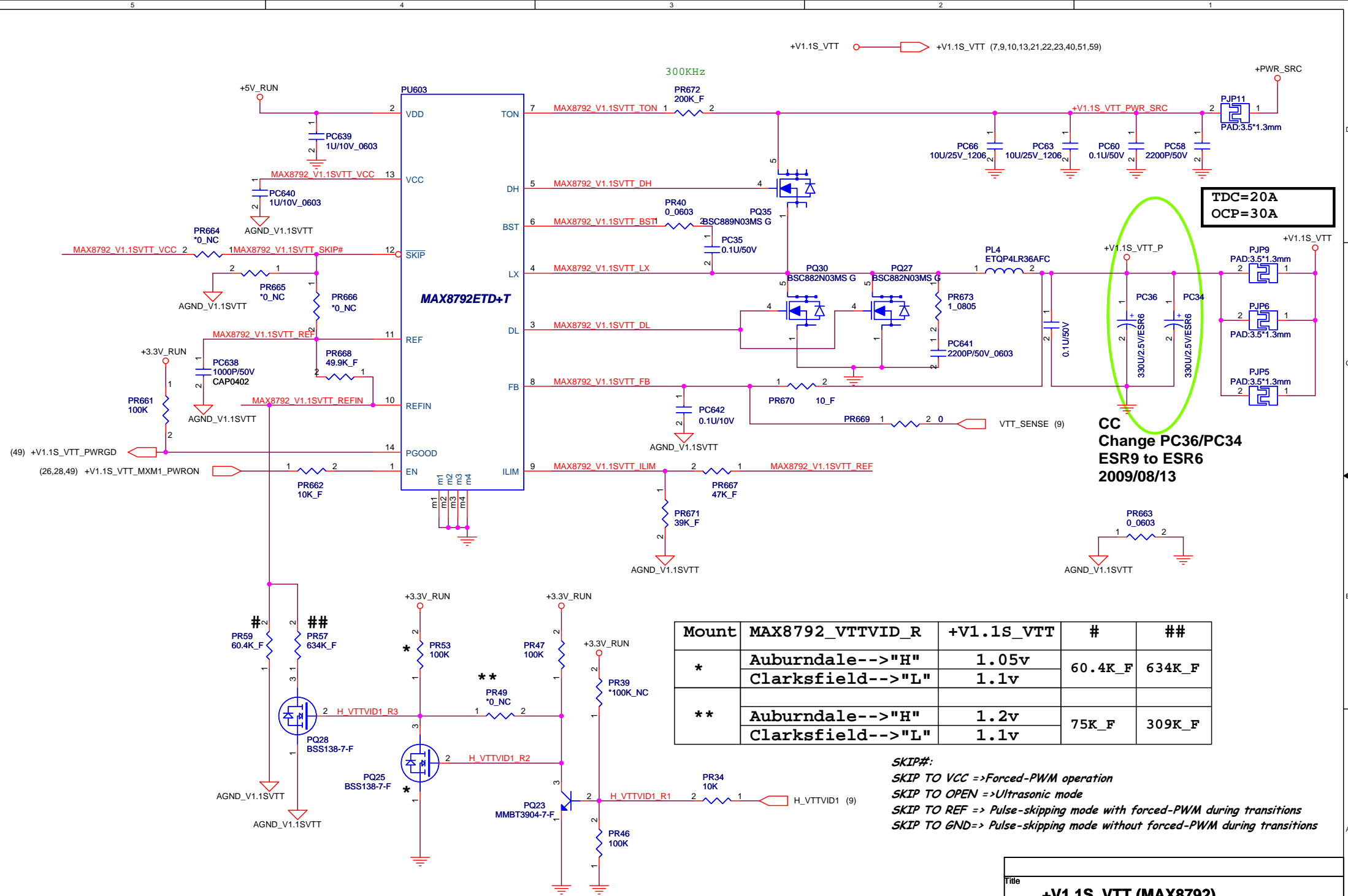
TDC=48Amax  
OCP=89A

Boost voltage

CC  
Change to mount such as PU601A,PR609, PR612, PR618...  
2009/08/13

GPIO1	GPIO2	Actions
0	0	Increase 150mV
0	1	Increase 75mV
1	0	VID Voltage (default)
1	1	VID Voltage (default)



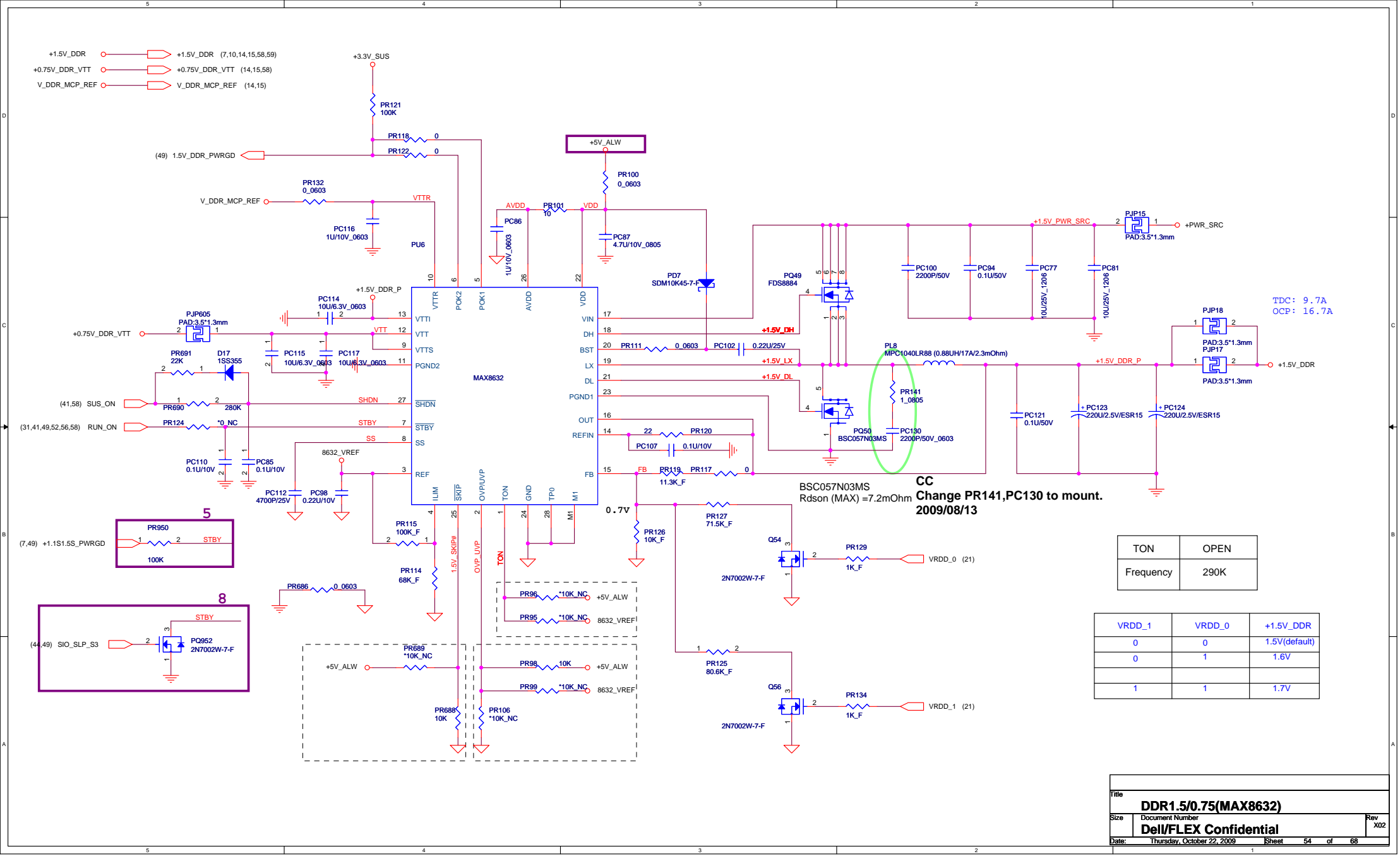


TDC=20A  
OCP=30A

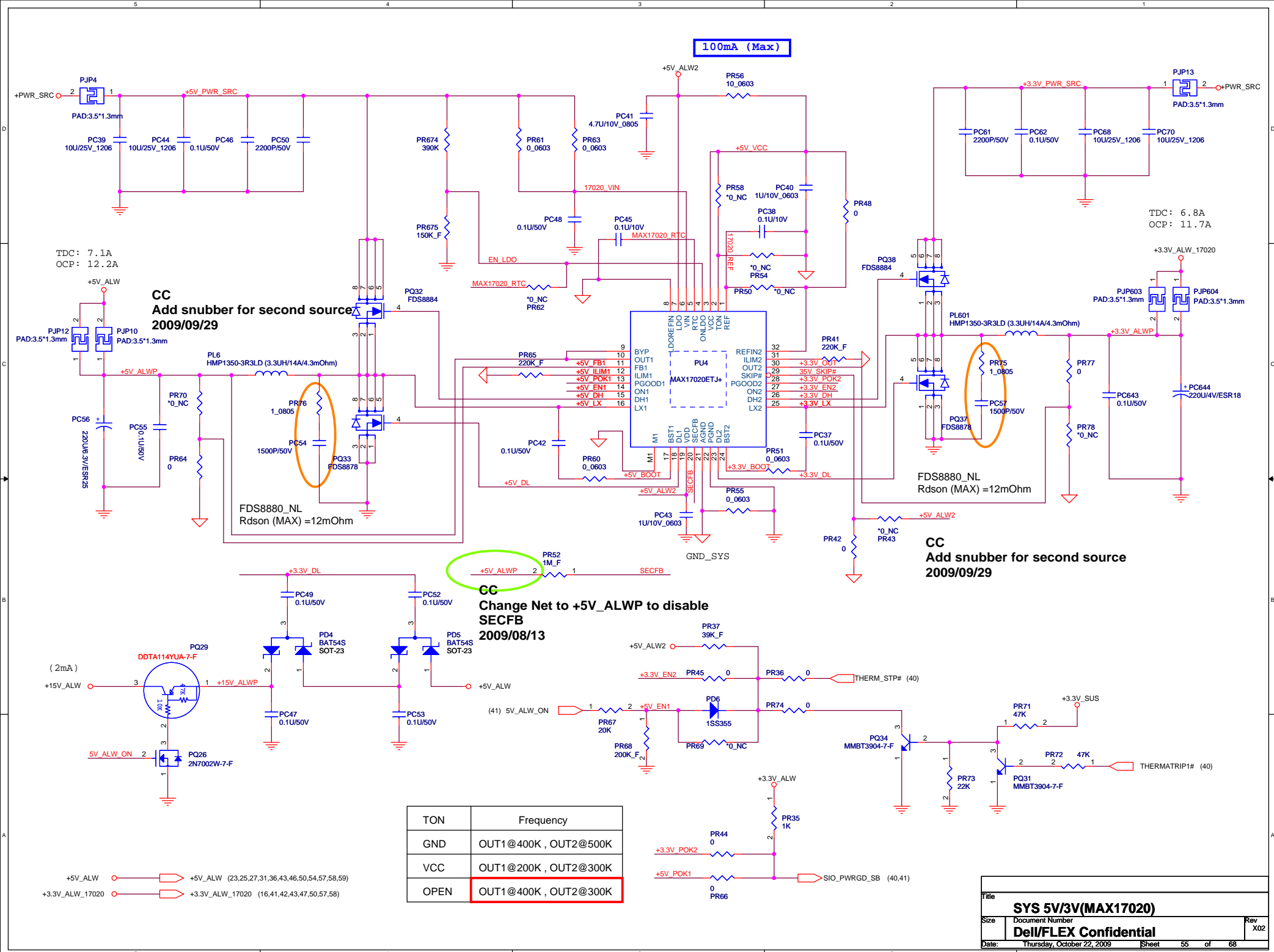
CC Change PC36/PC34  
ESR9 to ESR6  
2009/08/13

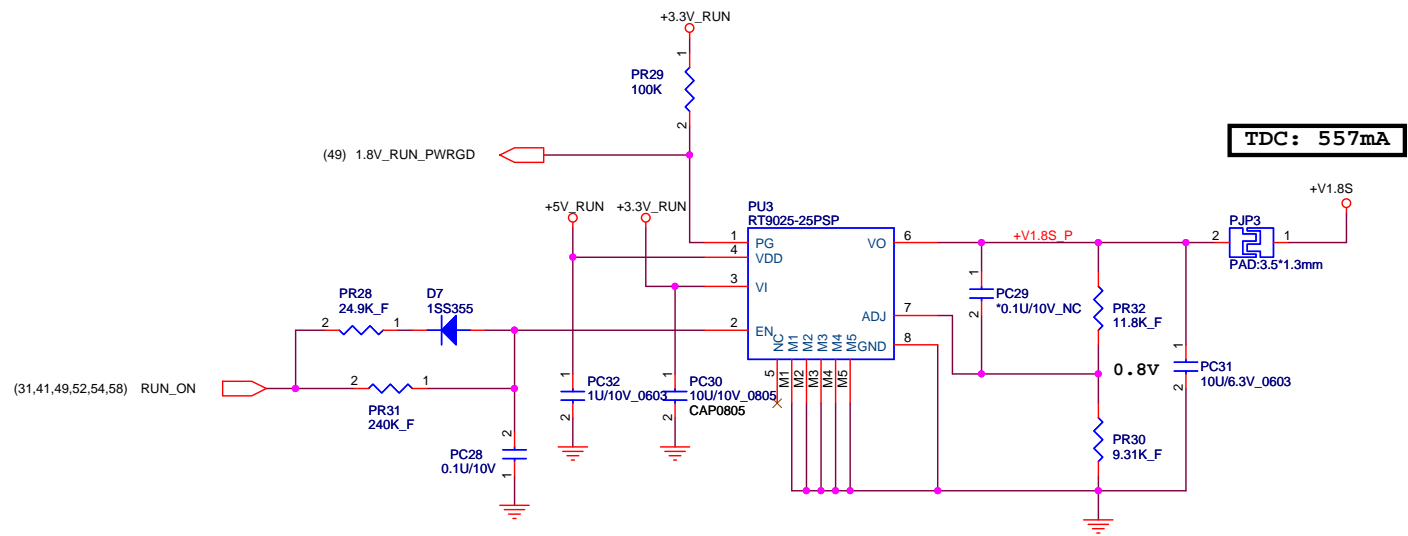
Mount	MAX8792_VTTVID_R	+V1.1S_VTT	#	##
*	Auburndale-->"H"	1.05v	60.4K_F	634K_F
	Clarksfield-->"L"	1.1v		
**	Auburndale-->"H"	1.2v	75K_F	309K_F
	Clarksfield-->"L"	1.1v		

SKIP#:  
SKIP TO VCC => Forced-PWM operation  
SKIP TO OPEN => Ultrasonic mode  
SKIP TO REF => Pulse-skipping mode with forced-PWM during transitions  
SKIP TO GND=> Pulse-skipping mode without forced-PWM during transitions

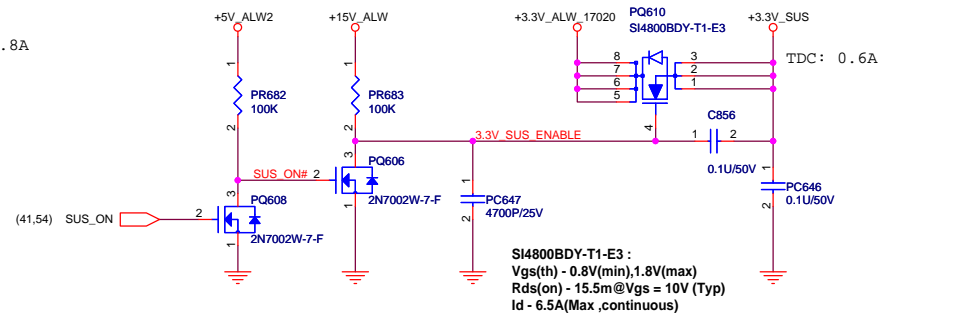
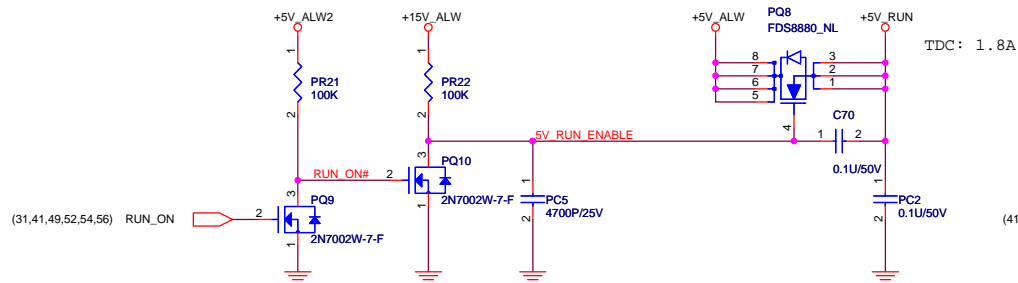




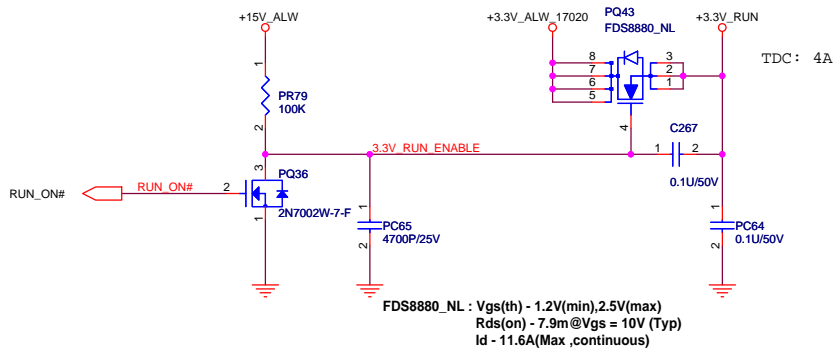
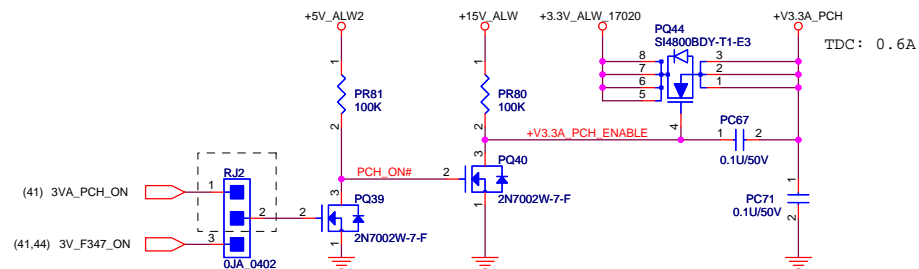
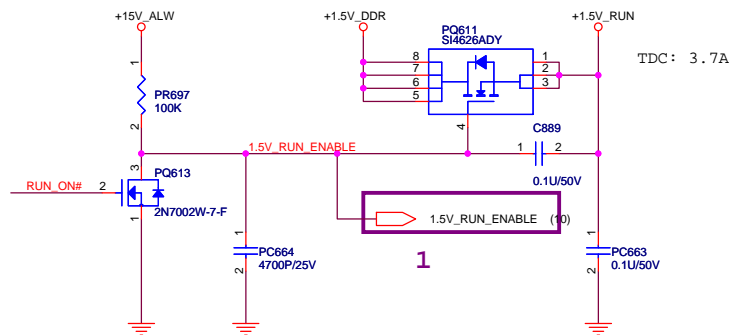




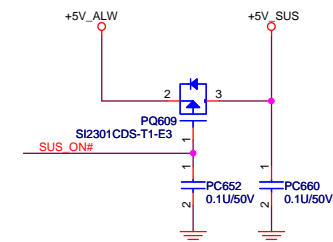
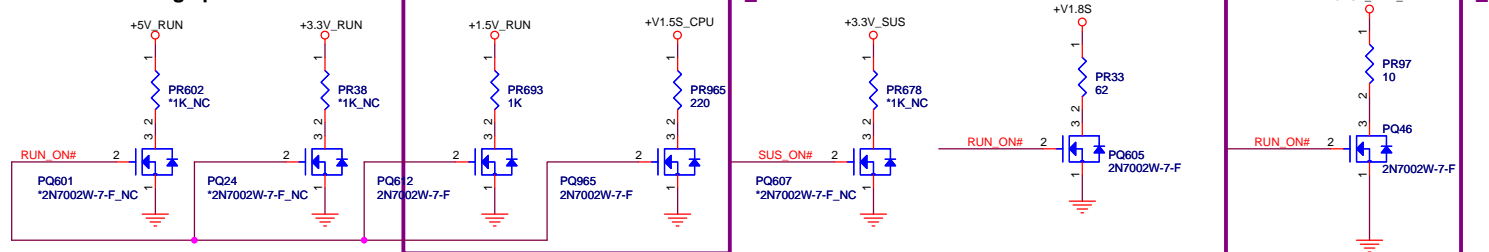




SI4336DY-T1-E3 :  
Vgs(th) - 1.0V(min), 3.0V(max)  
Rds(on) - 2.6m@Vgs = 10V (Typ)  
Id - 17A(Max ,continuous)

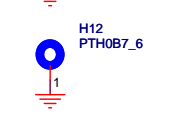
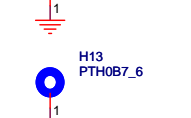
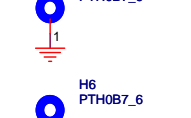
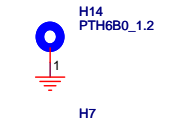
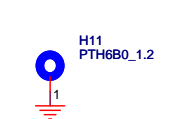
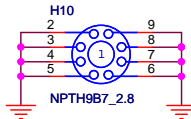
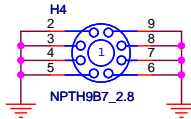
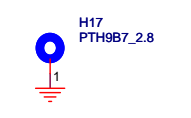
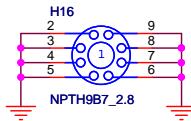
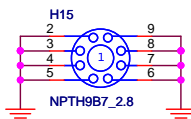
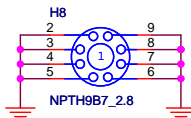
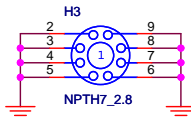
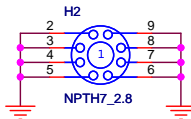
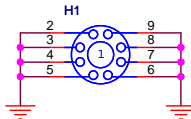
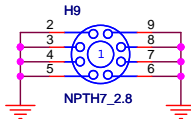
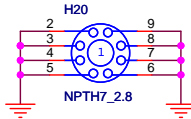
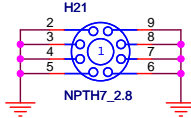
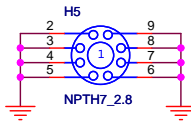


## Reserve discharge path



Title		
RUN POWER SW		
Size	Document Number	Rev
	Del/FLEX Confidential	X02
Date:	Thursday, October 22, 2009	Sheet 58 of 68

Screw Hole
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FID

FID4  
 1 NC, NO CONNECT TO ANY.

FID2  
 1 NC, NO CONNECT TO ANY.

FID3  
 1 NC, NO CONNECT TO ANY.

FID1  
 1 NC, NO CONNECT TO ANY.

FID604

1 NC. NO CONNECT TO ANY.

FID602

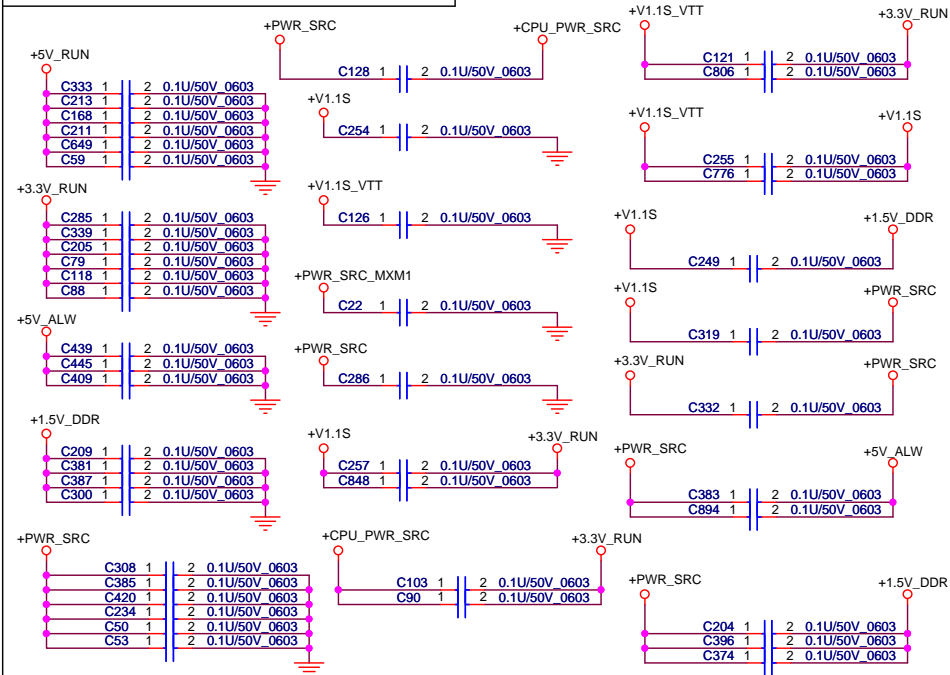
1 NC. NO CONNECT TO ANY.

FID603

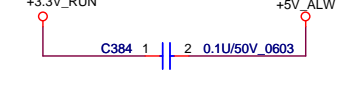
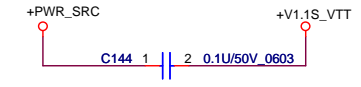
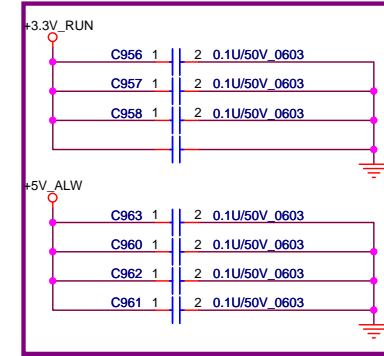
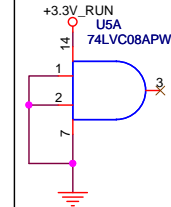
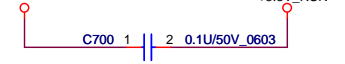
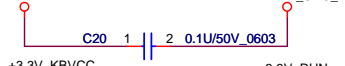
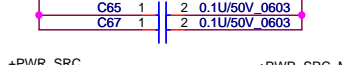
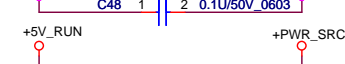
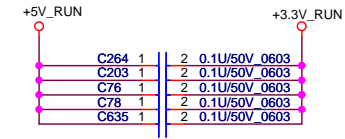
1 NC NO CONNECT TO ANY

FID601

1 NO CONNECT TO ANY



Moat Cap
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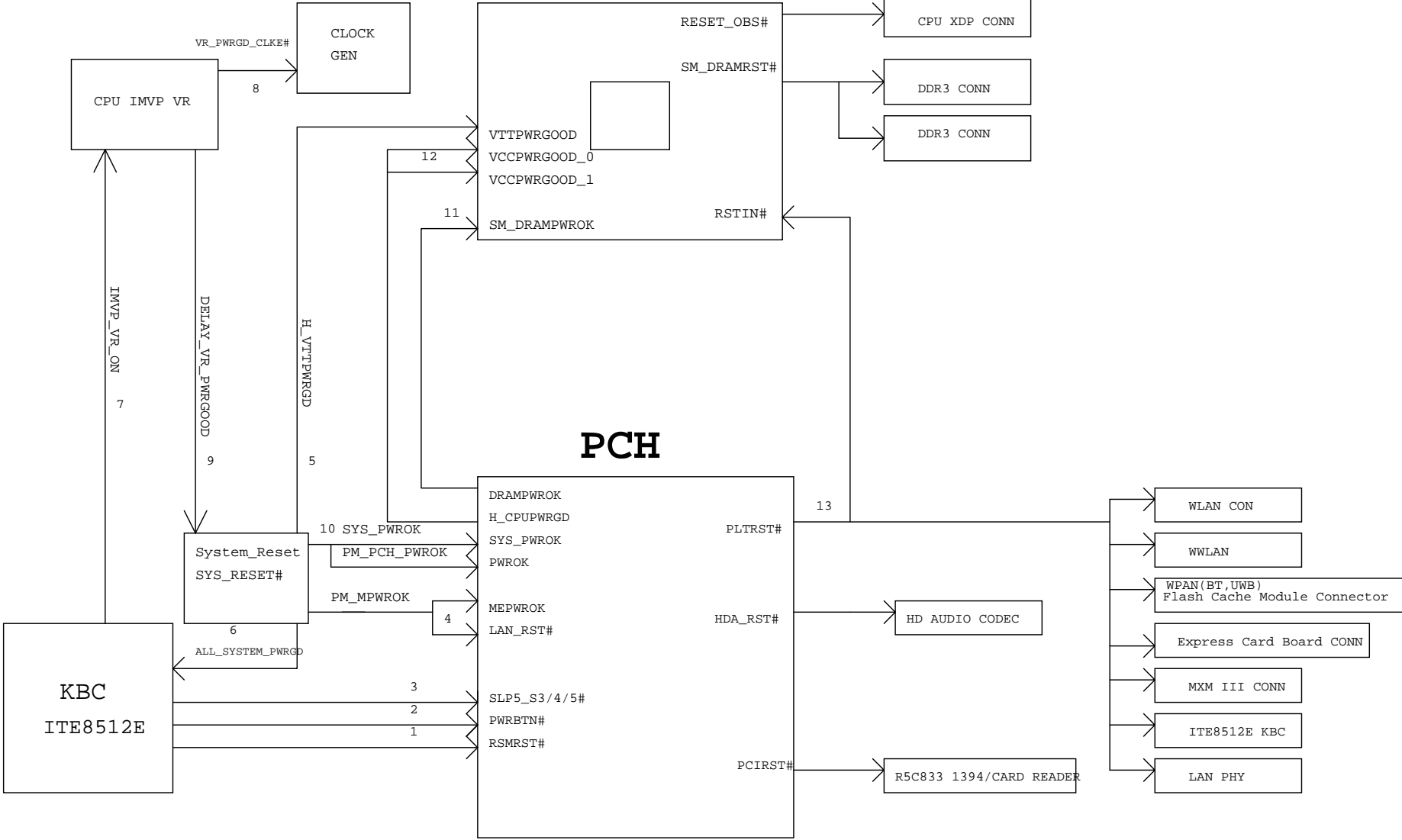




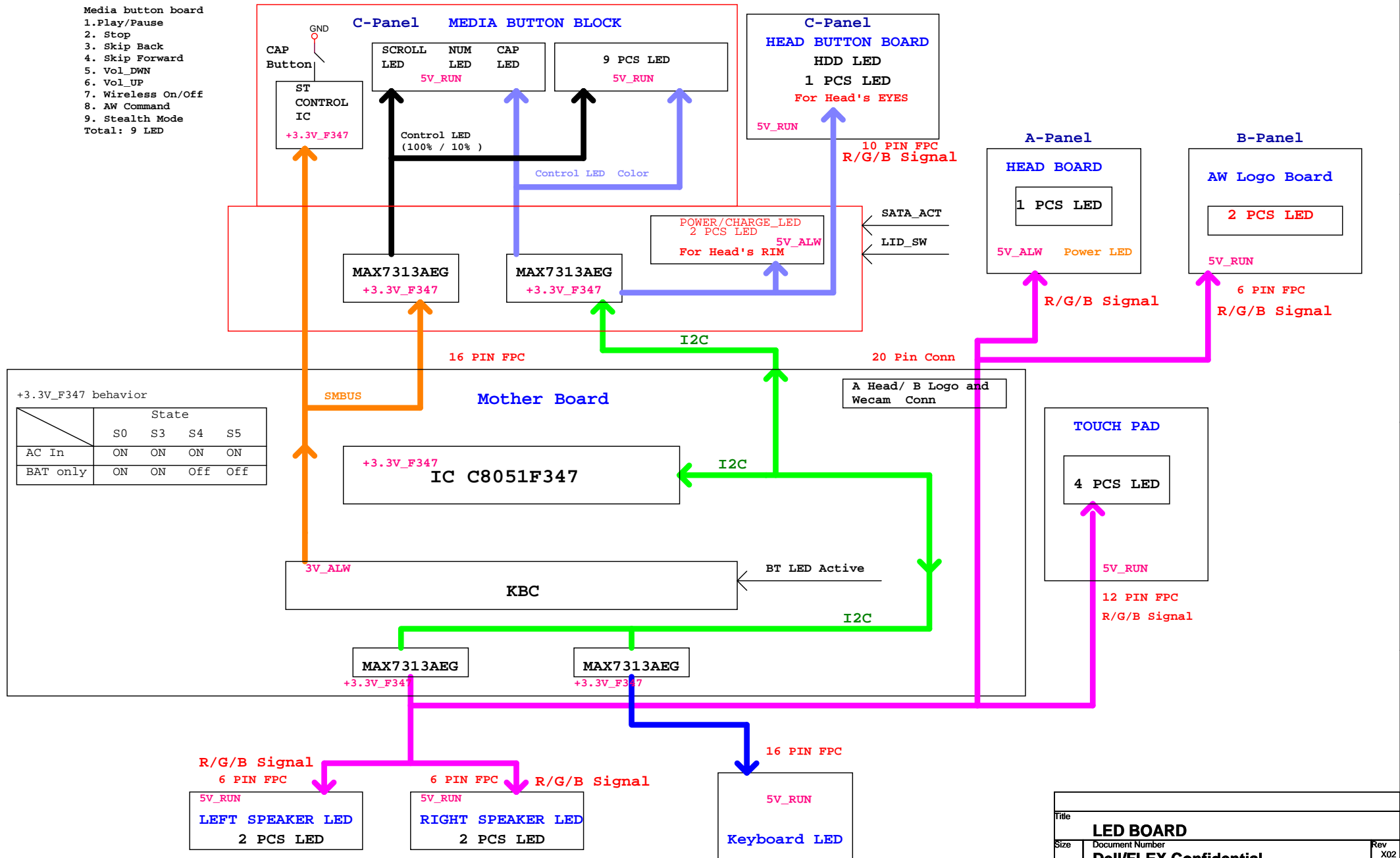
RESET MAP

CPU

PCH

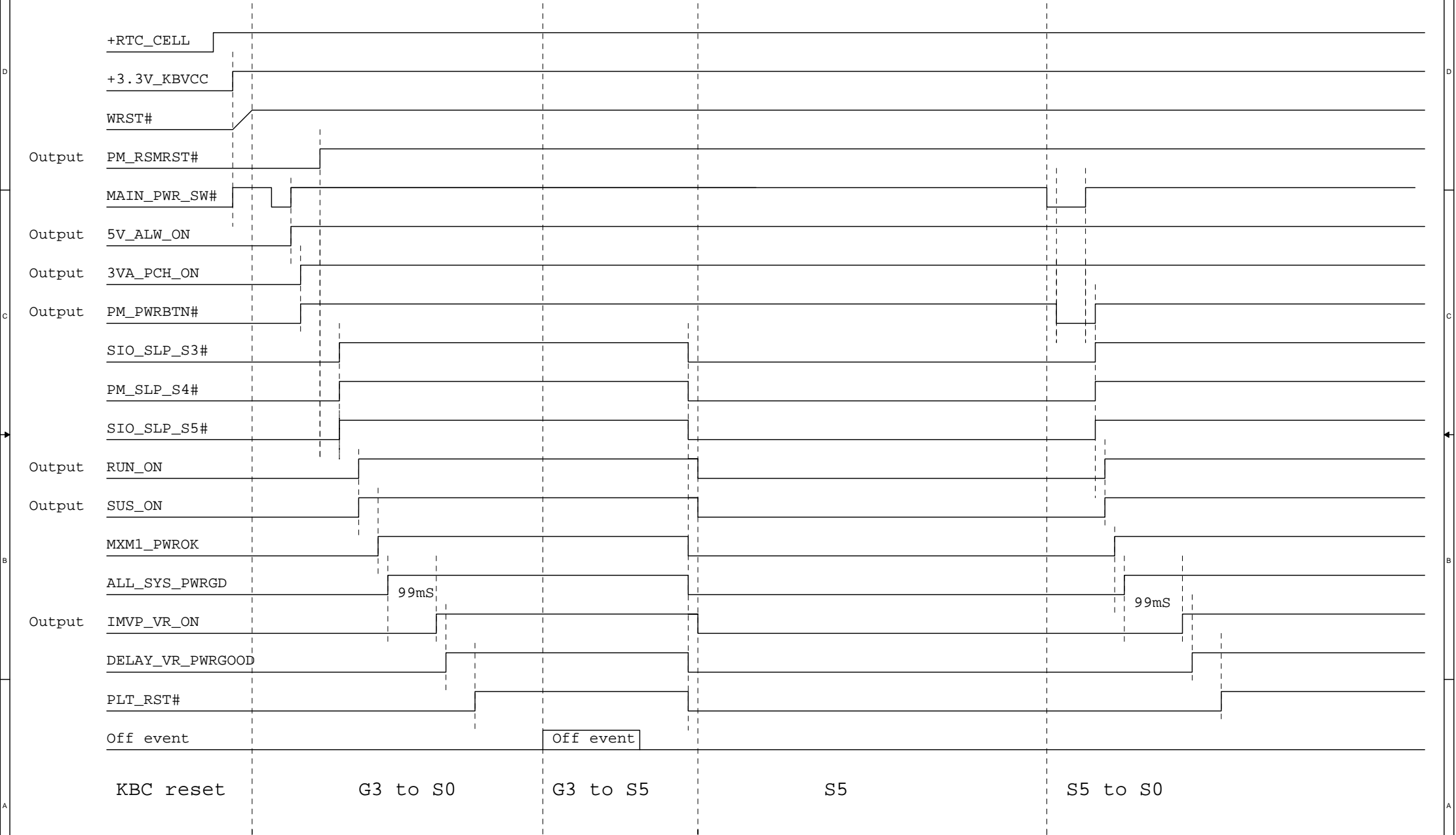


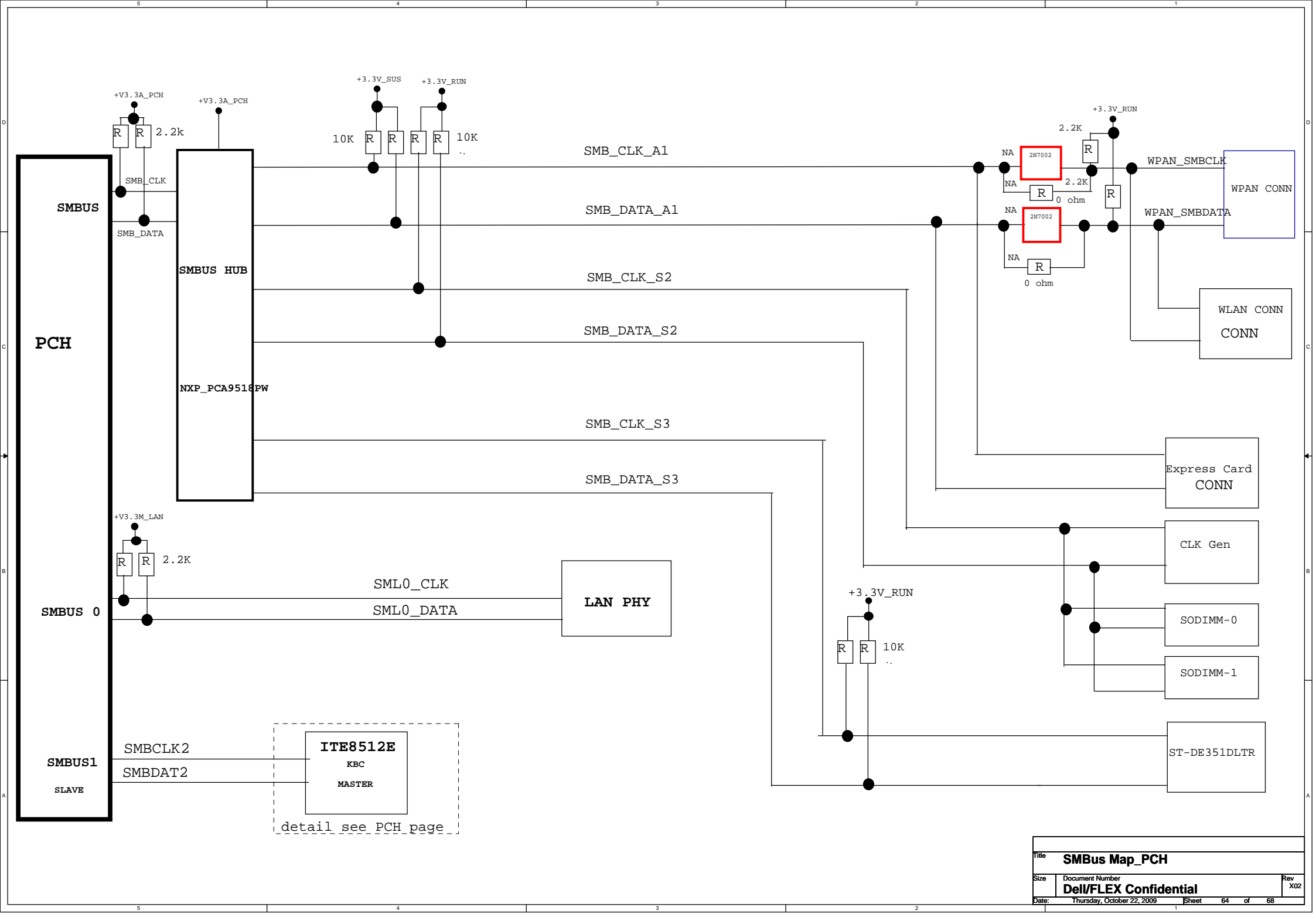
- Media button board
- 1.Play/Pause
  2. Stop
  3. Skip Back
  4. Skip Forward
  5. Vol\_DWN
  6. Vol\_UP
  7. Wireless On/Off
  8. AW Command
  9. Stealth Mode
- Total: 9 LED

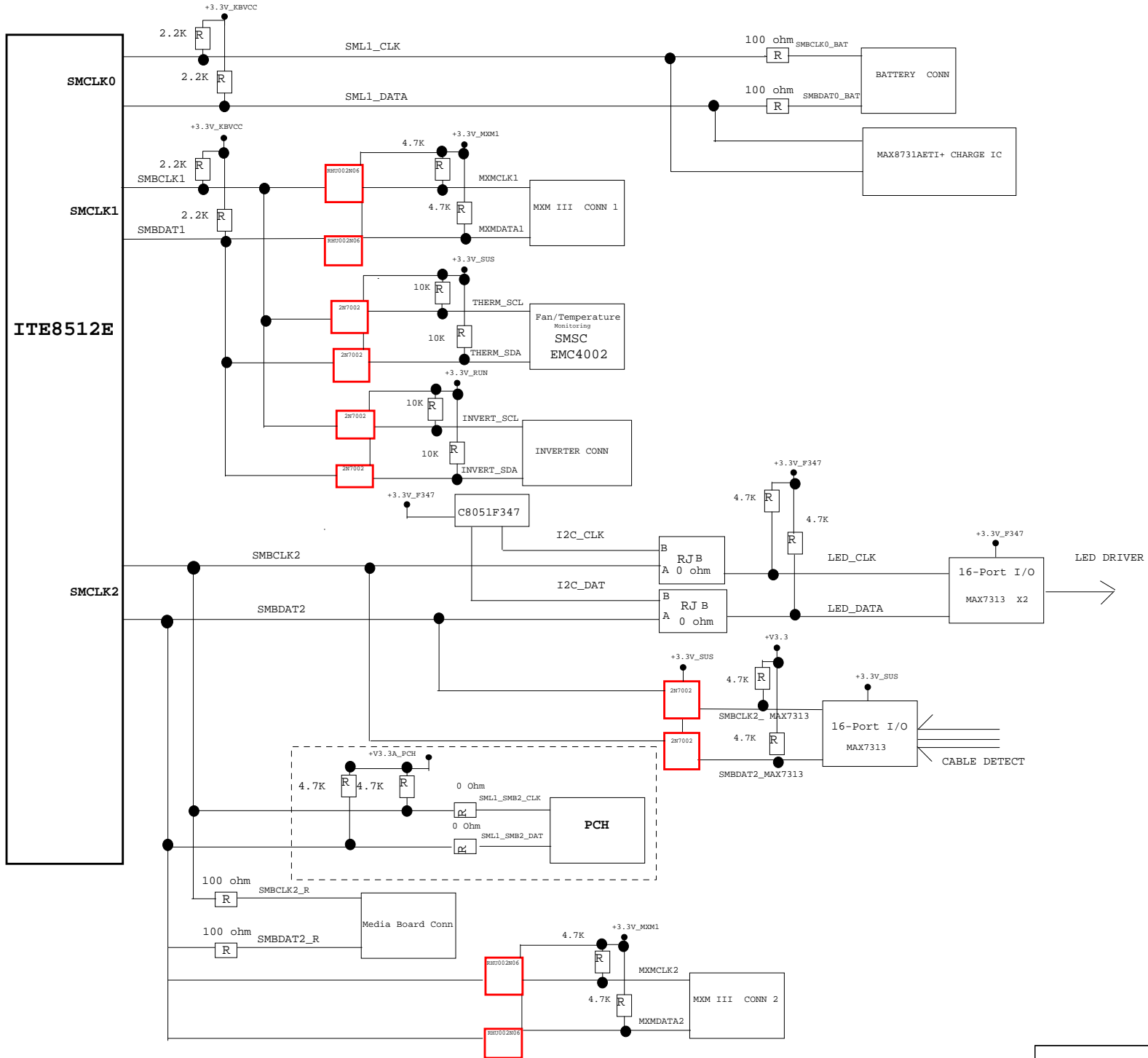




KBC Powre Up Sequence



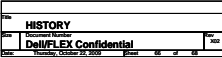




2009/02/18  
1. Add power solution, power link() modify power name +V56 ->+V5\_RUN, +V1.5S->+1.5V\_RUN, +V1.3S->+3.3V\_RUN, +V3.3->+3.3V\_SUS, +V5->+V5\_SUS...etc form CPU and Ibox)  
2. P.45 Add ONPT connector  
3. P.48 Change LAN to HANKEVILLE(R2577)  
4. P.1 Modify function block  
2009/02/23  
1. change EC connect  
2. Link USB line  
3. Change PCI\_GNT#0 to PCI\_GNT#8  
4. P.24 NVRAM power add a optional 1.8V sch, if ONPT used, using 1.8V  
2009/02/24  
1. change USB charger component  
2. Add some GPIO of PCH for Hybrid  
3. modify function block  
2009/02/26  
1. remove 2 DIMM  
2. add EDP connector  
3. remove P.50 original power sequence of QS and modify power sequence P.63 than copy to P.50  
4. modify LAN chip link p.48  
2009/02/26  
1. modify the power link from LAN chip to transform and RJ45  
2. modify some GPIO pin of P.68  
2009/03/04  
1. remove HYBRID switchable graphical card schematics  
2. remove VGA power of processor and FDI bus for delete UMA support  
2009/03/05  
1. change SIM slot to WIMAX connector  
2009/03/06  
1. add PCI-E switch schematics  
2009/03/10  
1. modify MDM and system power sequence  
2. add PML\_SLP\_S5 Rtc to U42  
3. p.3. p.4 description  
2009/03/13  
1. modify USB nets name from MCH to PCH  
2. modify 3904 L1B of P.40  
3. add MDM1\_PWOK and MDM2\_PWOK pull high  
2009/03/16  
1. modify power for placement  
2009/03/17  
1. modify p. 37, HSD, ODD power controller sch  
2. modify MDM1\_PRESENT to fit Defiant design  
3. change to eDP connector to 4 channel  
2009/03/19  
1. modify p. 23 GPIO  
2. modify HSD schematics of HDMI  
3. modify p. 55 3.3V power schematics  
4. modify p. 56 2.5V feedback resistor  
5. add 1.1V dis-charged  
2009/03/20  
1. modify power p. 51 and p. 57  
2. add a reserve pull high resistor at MDM\_TSHD  
3. complete PCI-E switch schematics  
2009/03/23  
1. delete P39, R383,R452 and P.38, R380,R416 for dual pull high.  
2009/03/24  
1. LAN\_CLK\_BROK\_R with two power source pull high, remove one  
2. p. 19 SMBus HUB schematic modify, change mini PCI-E card to channel 4 to separate different power plan with the same channel, and add channel 3 pull high  
3. move C1135, C1136, C1138 to p. 64  
2009/03/26  
1. add 0-sensor at p. 37  
2. combine +V1.1S and +V1.1S\_VTT with a power controller  
3. add CPU core boost voltage function at p. 52  
4. SMBCLK2 and SMBDAT2 with dual pull high resistor, remove one.  
2009/03/30  
1. Add jumper between MDM and power  
2. remove +3.3V\_MDM2 power and modify +3.3V\_MDM2 to +3.3V\_MDM1  
3. CLK\_PCH\_SRC1\_N from AK47 of IBOX was wrong, change to CLK\_PCH\_SRC0\_P  
4. MDM master, DS\_HPD\_RSM signal remove AND-gate  
5. modify MDM1\_PRESENTN schematic from MDM connector, original with logical gate to SN7002  
2009/04/02  
1. remove mini card 3 and SIM card  
2. change P07 power plan from run to sus  
3. delete p. 60 all most atch cap.  
4. integrate TTL logical to reduce the quantity  
5. modify +3.3V\_ALW to connect to +V3.3A\_PCH  
2009/04/14  
1. modify the schematics to MMD V.3  
2009/04/19  
1. change the power controller in +V1.1S and +V1.1S\_VTT to MAX8792  
2009/04/20  
1. arrange the page number  
2. modify the block diagram, frontpage and add smbus map and EDC power up sequence  
3. modify the SMBus of Winax and BT connector as Defiant  
2009/05/22  
1. modify express card connector definition to differentiate the QS, MLX express card daughter board need to modify. In order to avoid the QS DB enter MLX or MLX DB enter QS, change the pin definition to cut the card reader power.  
2. separate MDM2 power  
3. change IR power plane to +3.3V\_ALM\_17020 because of +V3.3A\_PCH will be cut when shut down in battery .mode  
4. remove TPM and thermal IC un-used part  
5. modify US.18 pin VDD\_PWRMD design  
6. add second SATA HDD redriver IC  
2009/06/30  
1. P51 AGNDC net was not connect to system GND, change AGNDC to GND  
2. P39 change PCI-E latch connector to SCREEN part  
3. change U21 pin UD000 to PCI-E clock repeat  
2009/07/02  
1. change U17 part because Capella do not need combine the BIOS into EC flash  
2. correct power P0605 schematics  
2009/07/06  
1. Add EMI stitching CAP  
2009/07/08  
1. Add CPT DUAL PI filter and by-pass CAP for EMI  
2009/07/09  
1. reserve ICS91A83185 co-layout schematics for over-clock function  
2. change MDM output configuration to below

MLK Define	For NV			For AMD	
	N10E-GTX1	N11E-GTX1	N11E-GS1/GE1	M98	Broadway
DPA	HDMI *	HDMI	HDMI	HDMI	HDMI
DPB	No Function	No Function	No Function	No Function	No Function
DPC	No Function	DP *	DP	DP	DP
DPD	No Function	eDP *	eDP	No Function	eDP

2009/07/11  
1. modify HDMI\_TX\*\_N and HDMI\_TX\*\_P  
2009/07/13  
1. rename



Item	Fix Issue	Reason to change	Rev	Page	Modify list
1 2009/08/4	S3 power reduce	S3 power reduce	X01	7, 10, 12, 21, 49, 54, 58	Intel cut off the +V1.5S_CPU power of CPU during S3, therefor , PM_DRAM_PWRGD_R and CPUDRAMRST# need to modify to controller by EC. Follow CRB's suggestion, the controller also need to reserve one from GPIO46 of PCH, original VRDD_1 need to change to GPIO15
2	HDD pin11	add spin-up delay schematic	X01	37	Using FFS_INT2_R of U7 signal to delay HDD spin-up
3 2009/08/5	S3 power reduce	S3 power reduce	X01	12, 41	find GPE1 of EC was not used, take the pin for S3 power reduce item controller
4 2009/08/10	S3 power reduce	Intel's review	X01	58	PR965 change to 220 ohm
5	HDD pin11	reserve the INT2 to PCH	X01	21, 37	add U7 int2 line to PCH's GPIO0 on P37 and P21
6	S3 power reduce	Intel's review	X01	14,15	RJ6 and RJ8 change to mounted B
7	over voltage of VCore	wrong schematics	X01	51	modify PU601.2 connect to PU601.1 directly
8	HDD pin11	wrong schematics	X01	37	modify Q953 and Q954 with wrong direction
9 2009/08/12	ELC controller	LED light on S4	X01	44	add RJ950 for S4 to ELC controller.
10	ONFI funtion remove	ONFI was not support	X01	22, 35	un-mounted J3, C448, R857, mounted R858
11	web cam power controller	reserve 7313 20pin	X01	41, 44	CAM_PWR_ON# change to output from U605
12	remove un-used EMI cap	remove un-used EMI cap	X01	48	remove C407, R413, C422, C424, C350, C426, R378
13	VCore overvoltage	X00 stage was not mounted	X01	51	Mounted PU601, PQ603, PQ604, PR606, PR620, PR612, PR618, PC608
14	Intel design guide	change the Cap with low ESR	X01	53	Change the PN of PC34, PC36
15	Power	High side Vds fail	X01	54	Mounted PR141, PC130
16	Power	Change Net to +5V_ALWP to enable SECFB	X01		Change the +5V_ALWP connect to PR52.2
17 2009/08/18	Power	Power fine tune and over voltage schematic's bom change	X01	55 51, 50,	Change PR679 value to 8.2k, change PR612, PR618 value to 309, mounted PR619, un-mounted PR621
18 2009/08/19	HDD pin11	change INT_2 connect	X01	21	change to GPIO48 of PCH connect to INT_2 of G-sensor
19	MXM2 power control	change the control signal from PCH to EC	X01	21, 41	MXM2_PRESENT#, MXM2_PWR_EN, MXM2_PWROK move to EC, add R973, R971, remove R799, R841
20 2009/08/20	Power	XMP over-voltage solution	X01	54	mounted PR127, Q54, PR129, PR125, Q56, PR134
21	EMI	change the by-pass resistor to choke of USB11	X01	31	un-mounted R43, R42, mounted L4
22	Power	to follow Clarksfield XE load line spec	X01	51	change PR607 to 5.23K
23	BID change to current value	change BID to PT stage	X01	21	mounted R720, un-mounted R721
24	LAN EA fail issue	modify the layout for LAN routing	X01	48	swap the pin assign of L34, L33 for routing
25	EMI	change the by-pass resistor to choke of USB2	X01	36	un-mounted R433, R434, mounted L38
26 2009/08/22	EMI	Modify RC priority of Media card interface	X01	46	Media card interface from U13 to CN15, original a Cap decoupling then damping a serious resistor change to damping a serious first, then a Cap add.
27 2009/08/25	remove ONFI	remove ONFI	X01	20	un-mounted R284
28	remove EEPROM of media card/1394	change to BIOS confige the controller	X01	46	un-mounted U10, R241. mounted R229
29 2009/08/26	Power	150W power support	X01	50	change PR138 to 10.7k for 150W power support
30	Slave VGA leakage issue	add power split component	X01	27	1. solve RST signal leakage: add a AND gate and R977, R976. 2. ACAV_IN signal leakage: sepearate MXM1 and MXM2, add Q956, R975, Q957 3. CLKREQ signal leakage: add Q958 to cut clkreq if MXM2 power disable. 4. combine THERM_MXM1#, THERM_MXM2# to THERM_MXM#, change GPA5 of EC(original THERM_MXM1#) to MXM_RST.
31 2009/08/27	EMI	add decoupling CAP for EMI	X01	59	+3.3V_RUN add C956, C957, C958, C959, +5V_ALW add C963, C960, C962, C961
32	power leakage	+5V_SUS leakage, change power source of PU6	X01	54	modify PR100 connect to +5V_ALW
33	power leakage	+V3.3M_LAN leakage	X01	47	add R981, R980, Q959 to split two power plane
34	power leakage	+3.3V_SUS leakage	X01	41	un-mount R113

Item	Fix Issue	Reason to change	Rev	Page	Modify list
1 2009/09/30	KB LED light uneven	different resistor value of the pin	X02	44	change R748 to 0ohm
2	VCore power	for second source used	X02	51	Change to mount PC16, PC17, PC622, PC19, PC14, PC13, PR650, PR646, PC636, PC619 for second source
3	charger		X02	50	change PL7, and mounted PR102, PC90
4	modify OCP	modify +V1.1S OCP value	X02	52	change PR88 value
5	3V/5V power	for second source used	X02	55	mounted PR76, PC54, PR75, PC57, change PR41, PR65 value
6	SI measure	add EMI solution will cause SI fail	X02	36	un-mounted L38 and mounted R433, R434
7 2009/10/2	over clock	change over-clock clock GEN	X02	5	change U3 to ICS3185, mounted L16, C139, un-mounted R88, R114
8	remove HDD2 redriver IC	SI could pass without re-driver IC	X02	37	remove C52, C51, C69, C68, U2, C54, C58, C61, C62, R50, R51, R52, R53, R54
9 2009/10/19	tuning the RTC timing	RTC timing will fail in some system in setup menu	X02	16	change C243 to 15pF
10	FDIM test fix	FDIM test fix	X02	9	change C768, C764, C650, C765, C766, C756, C186, C187, C192, C149, C150, C151, C152, C153, C154, C155 to 22uF, change PR634 to 255k ohm, change PC618, PC627, PC616 to 0.22uF/16V, Change PC623, PC617, and PC632 to mount,Change PC635, PC626, PC630, PC631, PC629, PC628 to 470uF/ESR4.5mohm.
11 2009/10/21	MXM2 power leakage	+3.3V_MXM2 with power leakage	X02	27, 28	add D953, D954, D955
12 2009/11/24	LAN LED	LAN LED will light if un-plug LAN and disable LAN function	A00	48	CN19.B1 change to connect to power, and CN19.B2 change to connect to R405.1

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